

# Model Name: GA-H77-D3H

1.0

SHEET

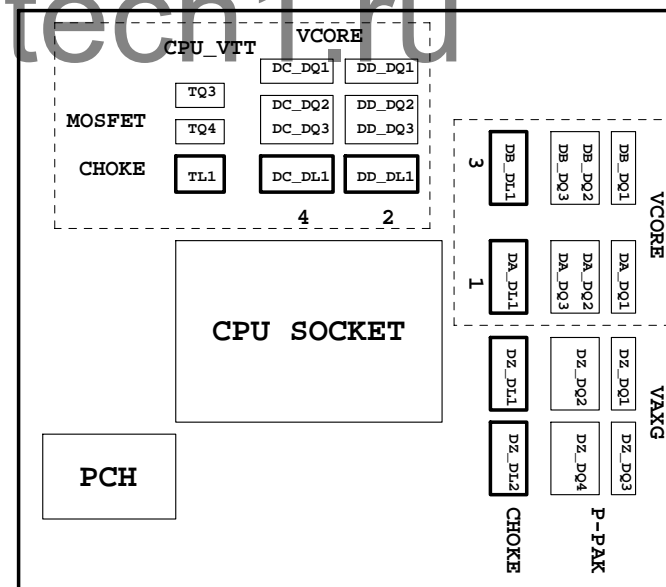
TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*3 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	VT2021 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564
24	VCORE PWM DRIVER IR3598
25	NCP3933 OVER VOLTAGE
26	DISCRETE POWER
27	DDR_15V & CPU_VTT PWM IR3570

SHEET

TITLE

28	DDR_15V & CPU_VTT PWM DRIVER CHL8550
29	VCCSA POWER
30	F_PANEL , F_USB2.0/3.0
31	ATX POWER, CLOCK GEN
32	HWM , KB/MS , FAN CTRL
33	LAN ATHEROS AR8151
34	N/A
35	M-SATA
36	DVI
37	HDMI , R_USB30
38	TABLE LIST
39	
40	



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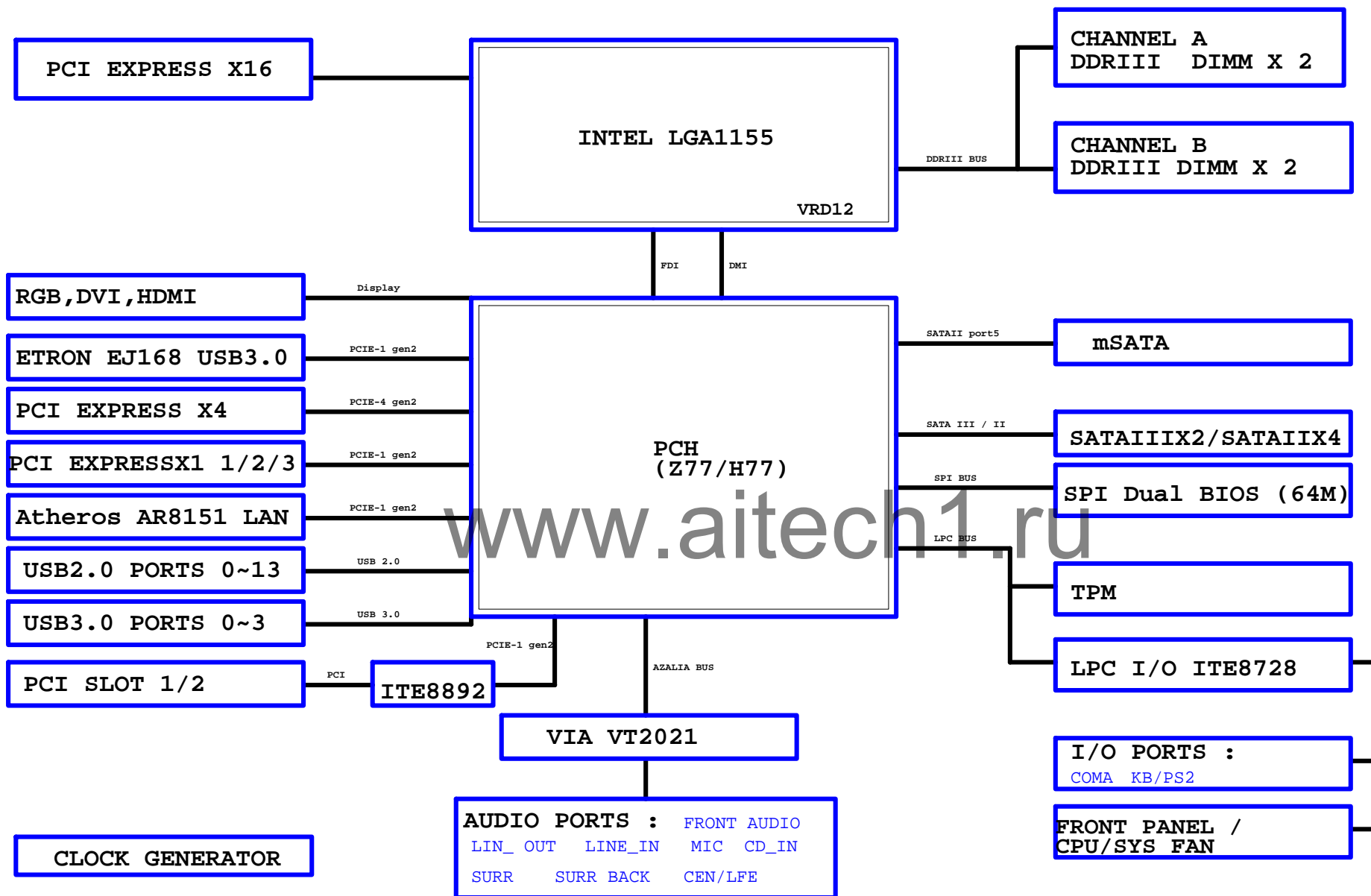
Cover Sheet		
Title	GA-H77-D3H	
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## Component value change history

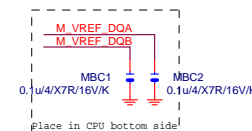
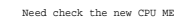
[illegible]

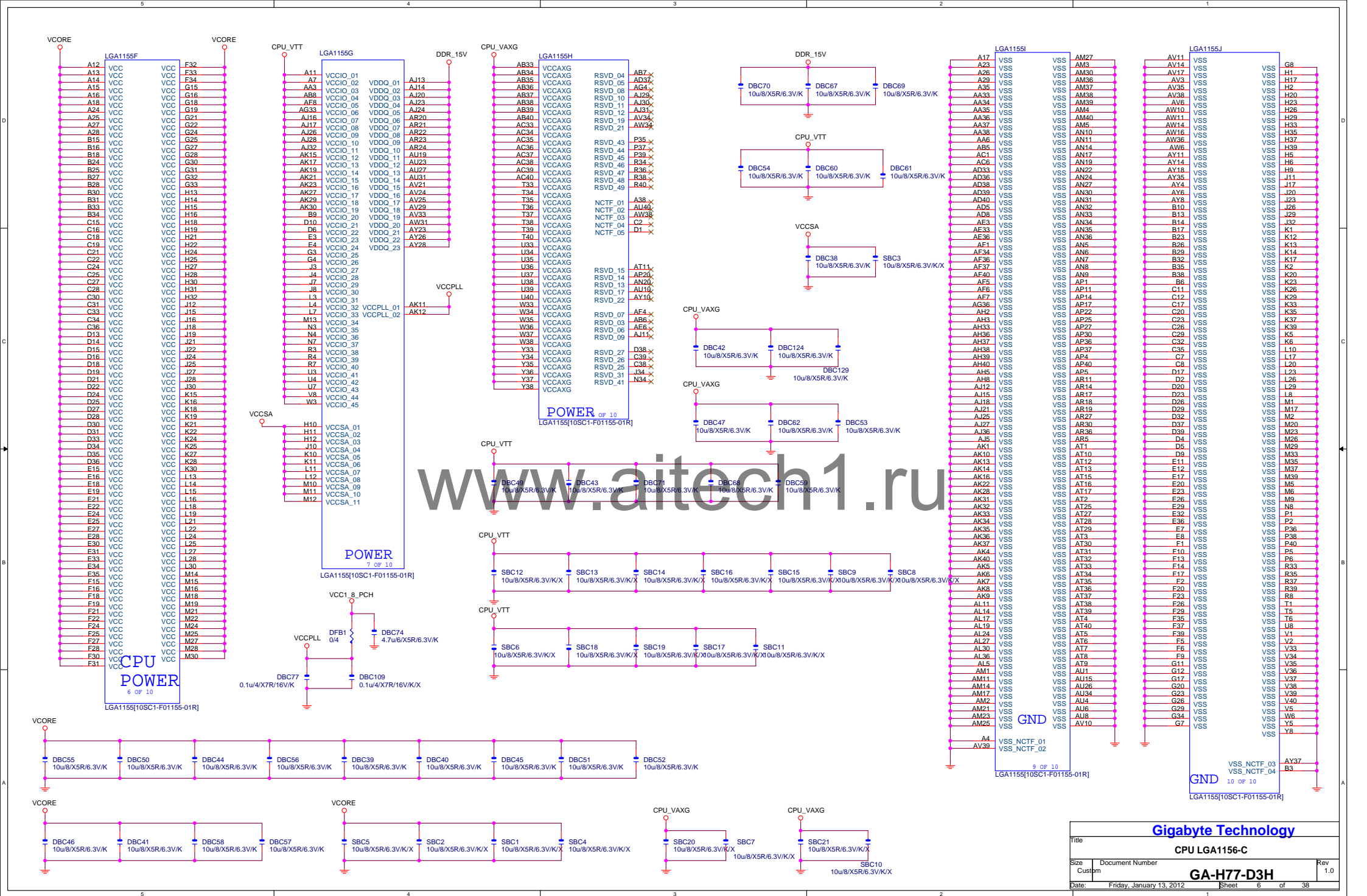
DATE	Change Item	Reason
P67X-UD3-B3		
2011/02/18-0.1	1. 移除LAR11 ,LAR14 , NR28 ,新增NTP11	
2011/02/18-1.0	2. 新增DR388,DR389,DR391 ; Remove DQ49,DR347,DR371 3. CR44改成R0603-RH 4. R1,LAR3,RBR20,LABC25 -->R0402-2-SHORT 5. RAQ1 --> Q_TO223-MASK 6. RARN1 --> R8P4R-0402-SHORT 7. CESD1-5 --> SSOP5 8. RAQ2,RAEC1一起往下移40mil 9. CESD2文字面要標pin1	
2011/03/8-1.01	1. Add "Dolby" logo	
2011/03/8-1.02	1. UAFB1,UAFB2,UBF1,UBF2 Footprint update 1206-->1812 2. Add "AD1" FOR 5VSB	
Z68XP-D3		
1.0	1. update MINI_PCIE footprint 2. 文字面 : SLOT部分全對齊	
Z77-D3H-0.1	EVT	
0.2-1216	1. Remove SS9172 , Add VCC3 內層(注意其他內層power,跨切割) 2. SPDIF AGND --> GND 3. PCI SLOT & PCIEK1/X4 CAP COST DOWN 4. 0 ohm --> SHORT PAD 5. REMOVE SMBUS FROM COMP TO SOLDER SIDE IN DR POWER 6. SATA3 connect Change to 90 degree (記得SATA3訊號部分要做挖空) 7. Add "108dB"文字面 8. Remove VCC1_05_PCH & VCC1_8_PCH gate net 9. Add EJ168 R_USB30_1 & F_USB3 10. UAE1/UAE2 NET SWAP 11. 內層+12V要打VIA在COMA處 12. SPDIFO_HDMI走12mil	
1.0	1. +12V內層加寬,0 ohm short排組留一個 2. SATA2-SATA3文字面要隱藏 3. NEC2/UAE3往右移,遠離PCH_HS 4. DART2 移至 DC_DQ1左上方 5. Q7 & DAR31 NET Change	

# BLOCK DIAGRAM







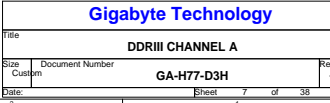


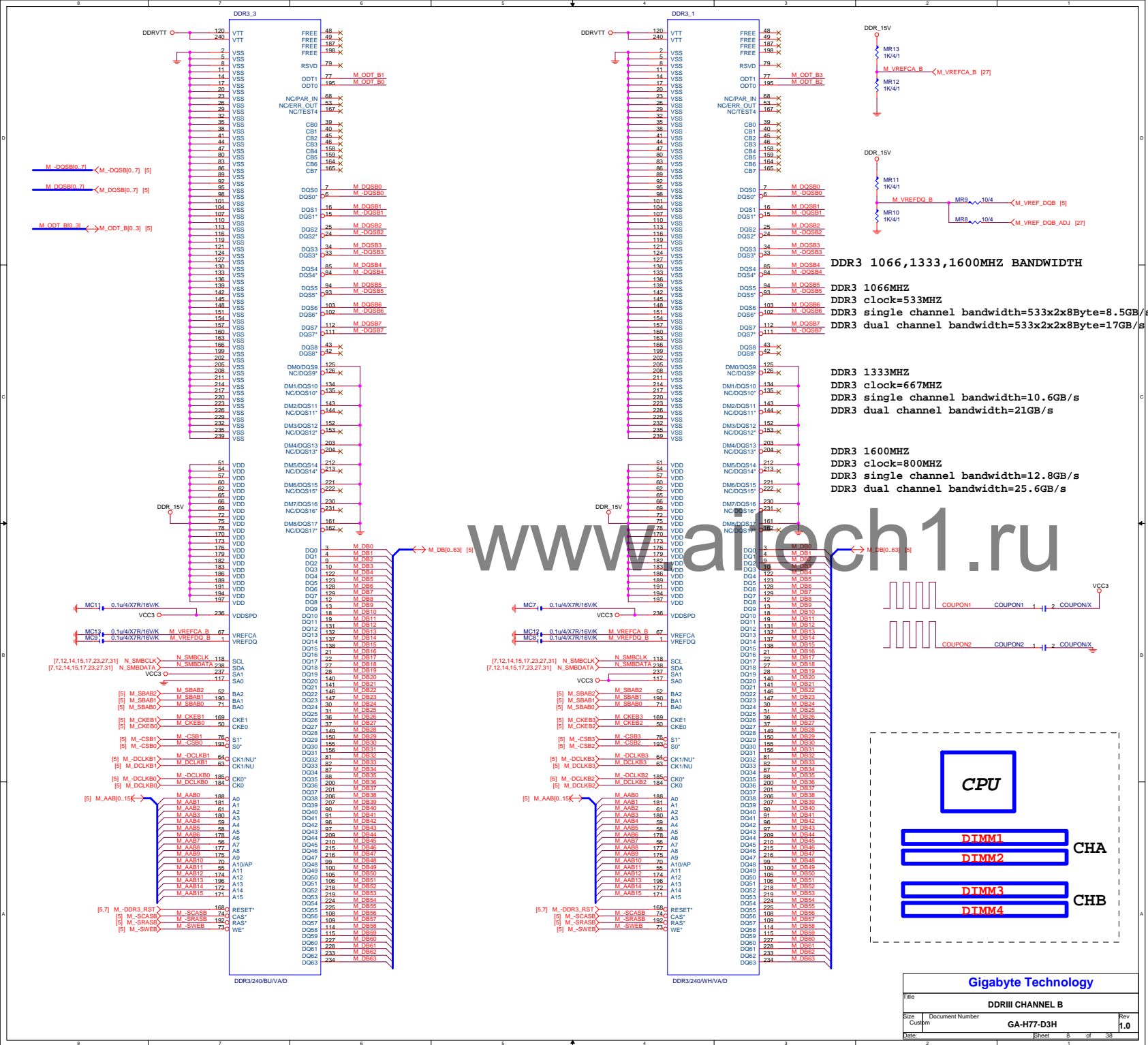
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CPU LGA1156-C

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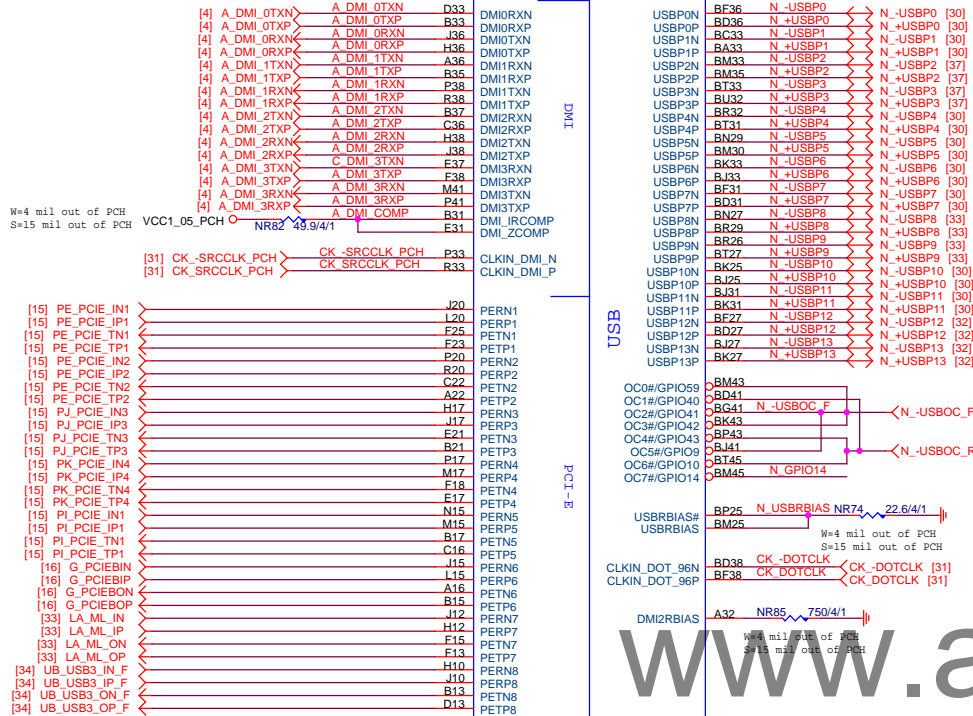
USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS  
Impedance=85 +- 17.5%  
Back Panel < 10000 MILS  
Front Panel < 6000 MILS

USB2.0 : 12/4.5/7/5/4.5/12 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%

PCBH

PCHG

FDILINK



OC[3:0]# for Device 29 (ports 0-7)  
OC[7:4]# for Device 26 (ports 8-13)

USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

FDI\_TXP0\_7I >>> FDI\_TXP0[0..7] [4]  
FDI\_TXN0\_7I >>> FDI\_TXN0[0..7] [4]

FDI:12/4/5/4/12  
Impedance=85 +- 17.5%

PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)  
Impedance=80 +- 17.5%

PCH\_HS

PCHE

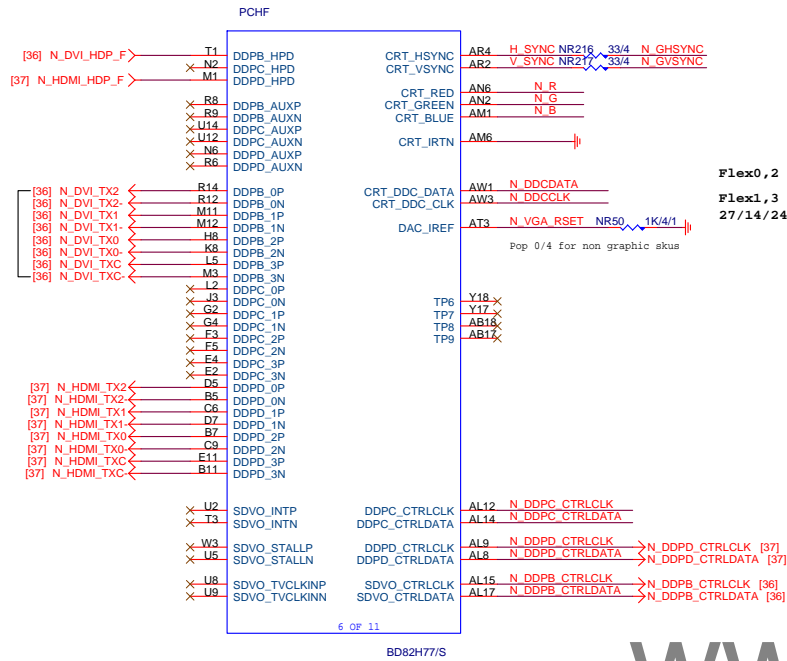
NVRAM

Mount for integrated clock Generation Mode

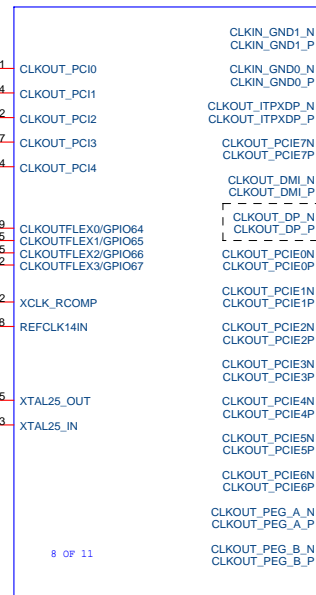
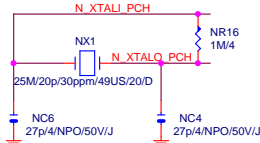
CK\_DOTCLK NR84 8.2K/4/X  
CK\_DOTCLK NR88 8.2K/4/X  
R102 short to GND in non graphic SKU

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Title		
PCH FDI,DMI,USB,PCI-E		
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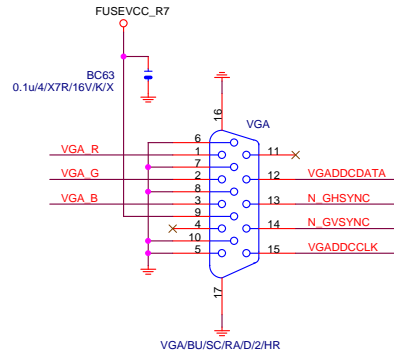
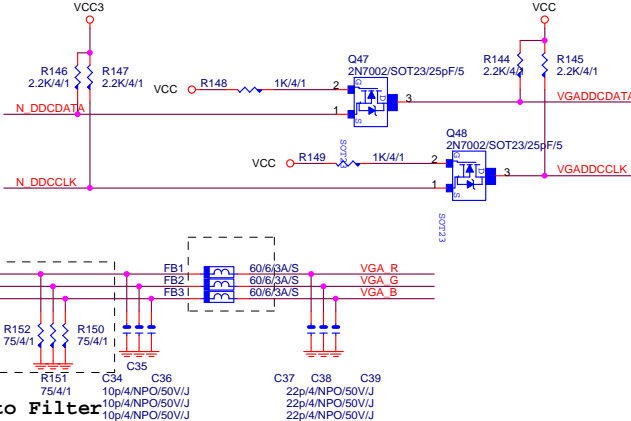
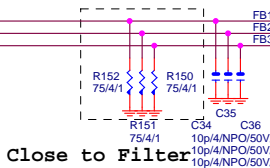
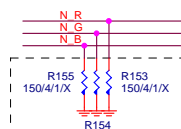
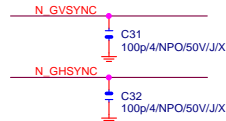
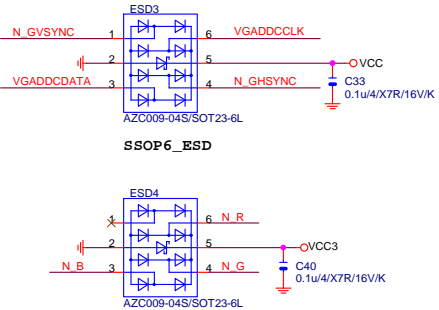
Flex0,2 : 33MHz  
Flex1,3 : 27/14/24/48/25MHz



Differential Clock: 18/4/6/4/18  
Impedance=90 +- 15%

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Check if NC for P67 non graphic chip

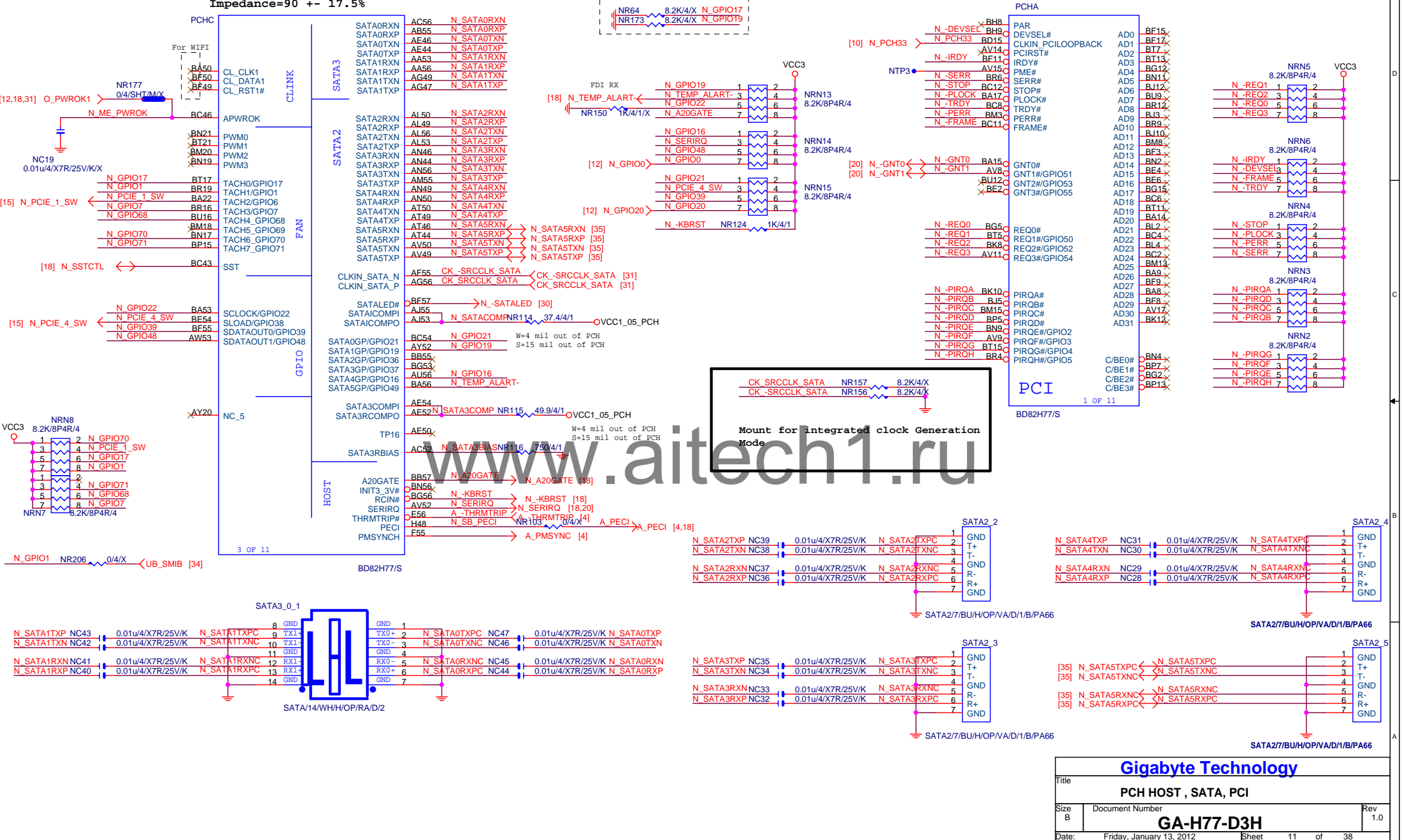


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Title			
PCH DISPLAY ,CLK BUFFER			
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SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%

SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%

MB-ID



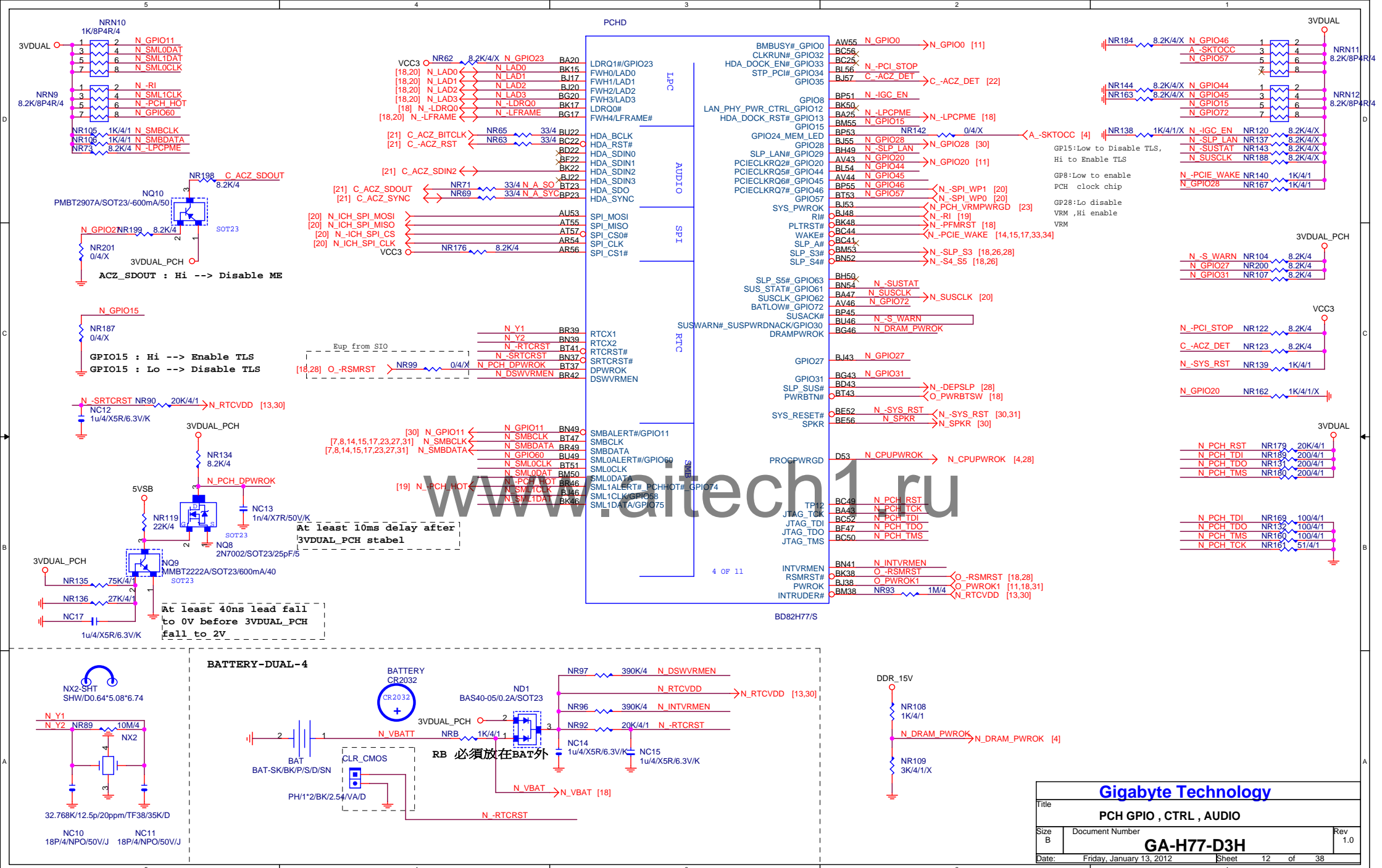
Gigabyte Technology

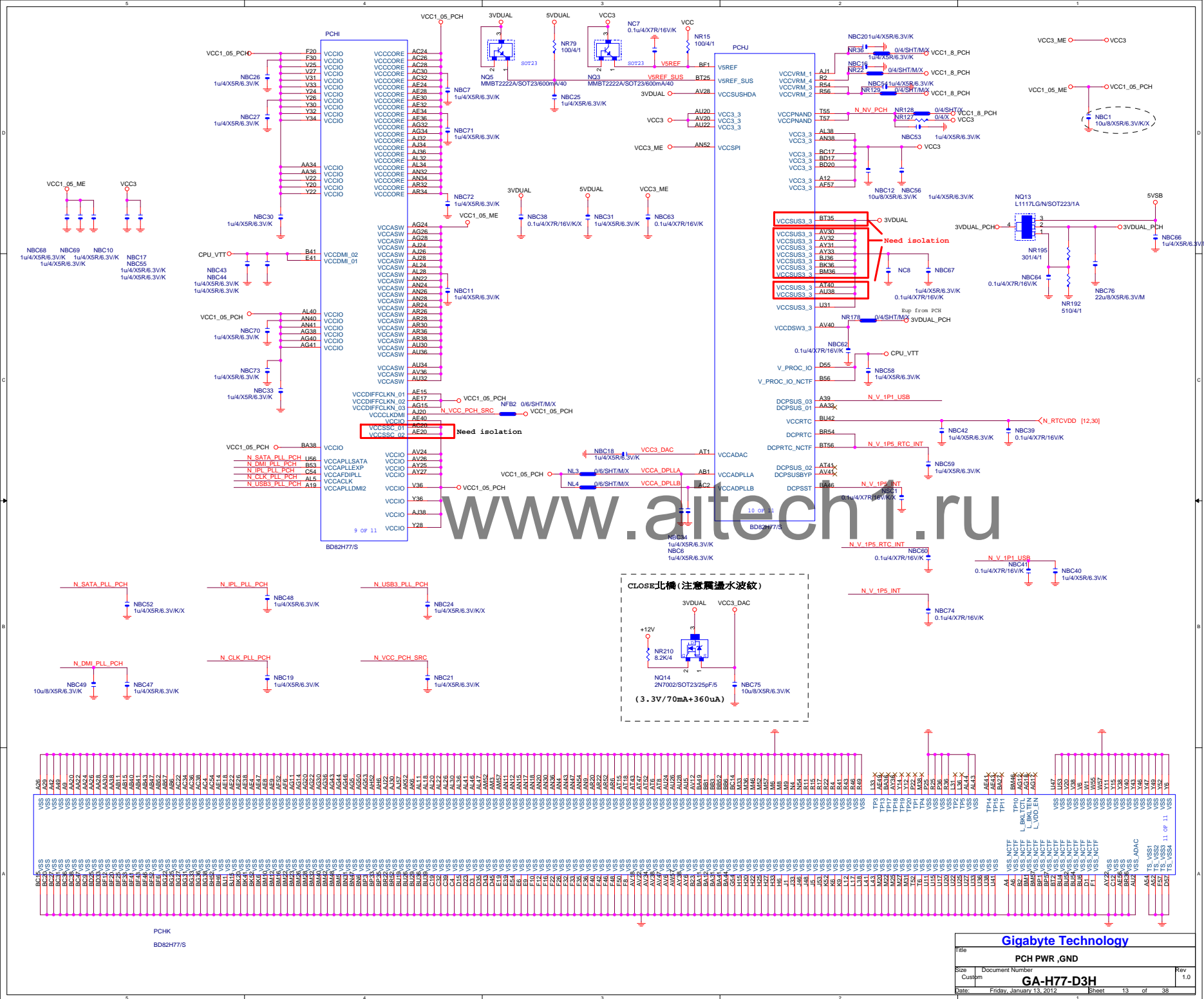
PCH HOST , SATA, PCI

GA-H77-D3H

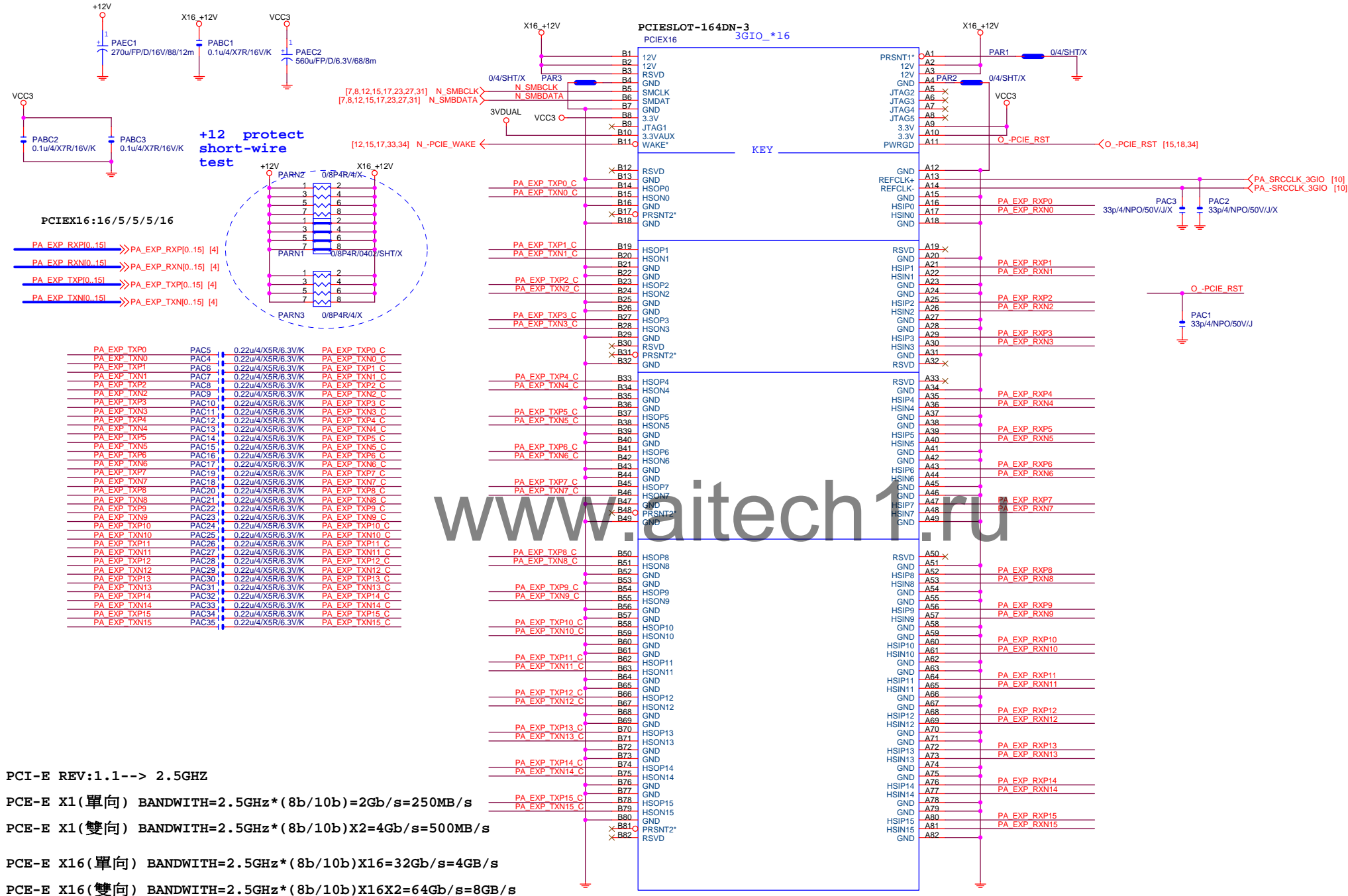
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PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

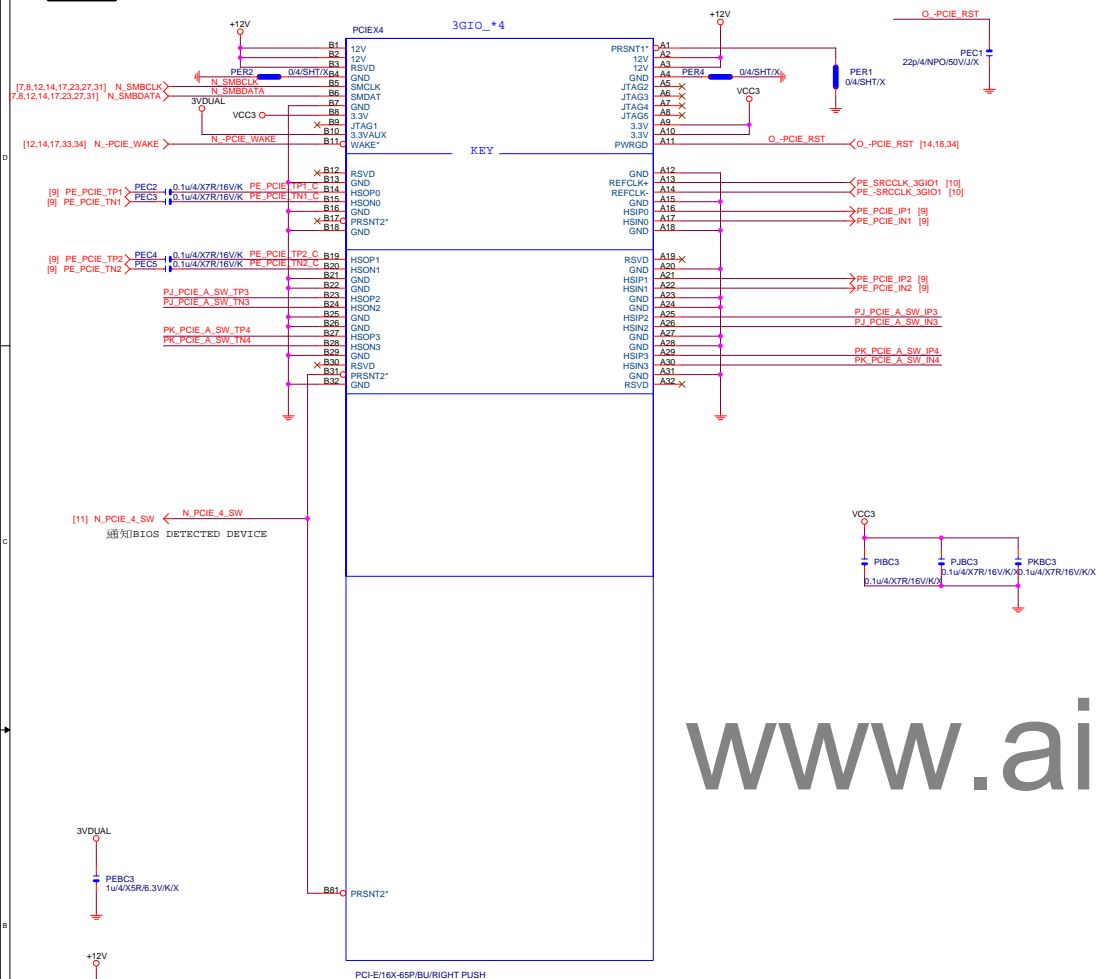
PCE-E X16(雙向) BANDWITH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

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PCI EXPRESS * 16			
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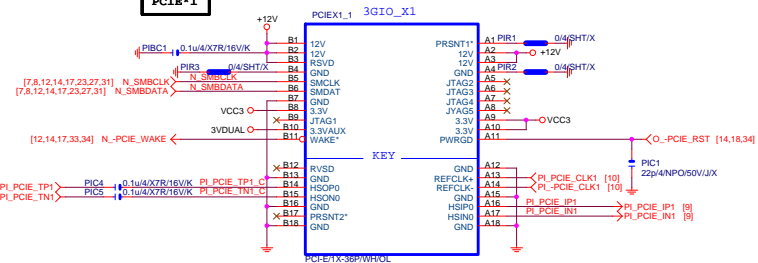


PCIE\*4

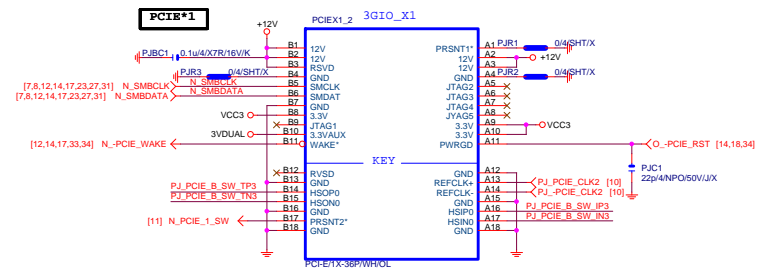


	N_PCIE_4_SW (PCH GPIO38)	PCIE_X1 (SIO_GPIO26)
PCIE_X1, PCIE_X4 --> X1 (Default)	H	H
PCIE_X1_2/PCIE_X1_3 Have devices PCIE_X4 --> X1	H	H
PCIE_X1_2/PCIE_X1_3 No devices PCIE_X4 Have devices PCIE_X4 --> X4	L	L

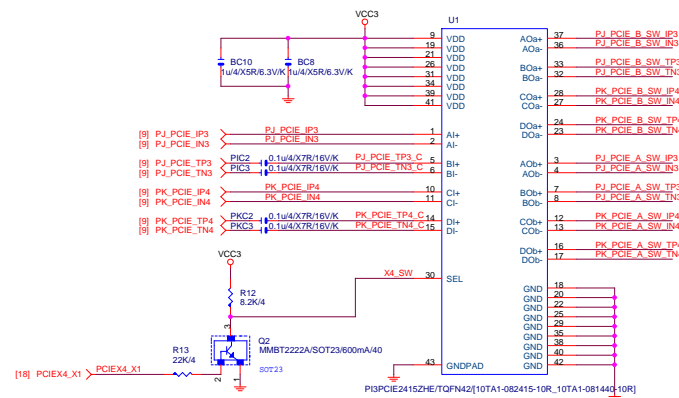
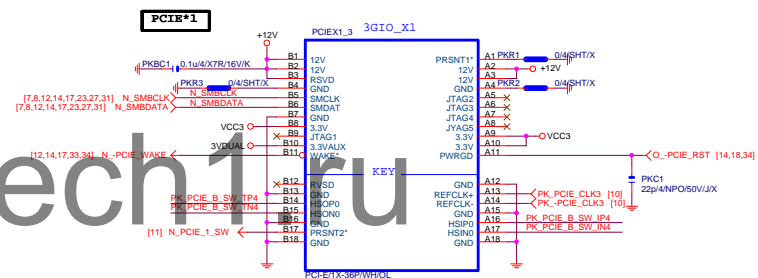
PCIE\*1



PCIE\*1



PCIE\*1



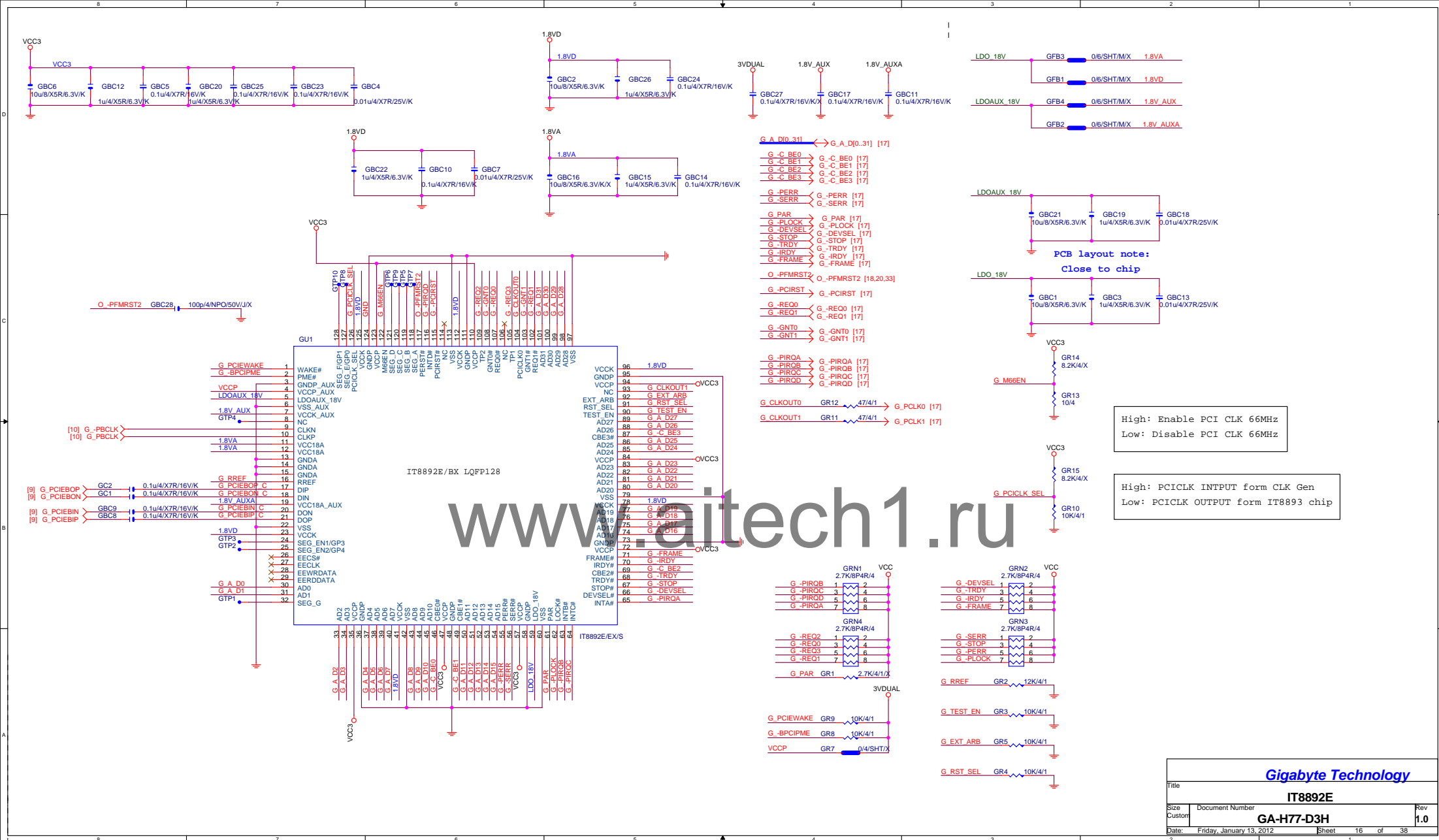
Function	SEL
X1--> x0a	L <sub>1</sub> PCIE_X4 SLOT-->X1
X1--> x0b	H <sub>1</sub> PCIE_X4 SLOT-->X4

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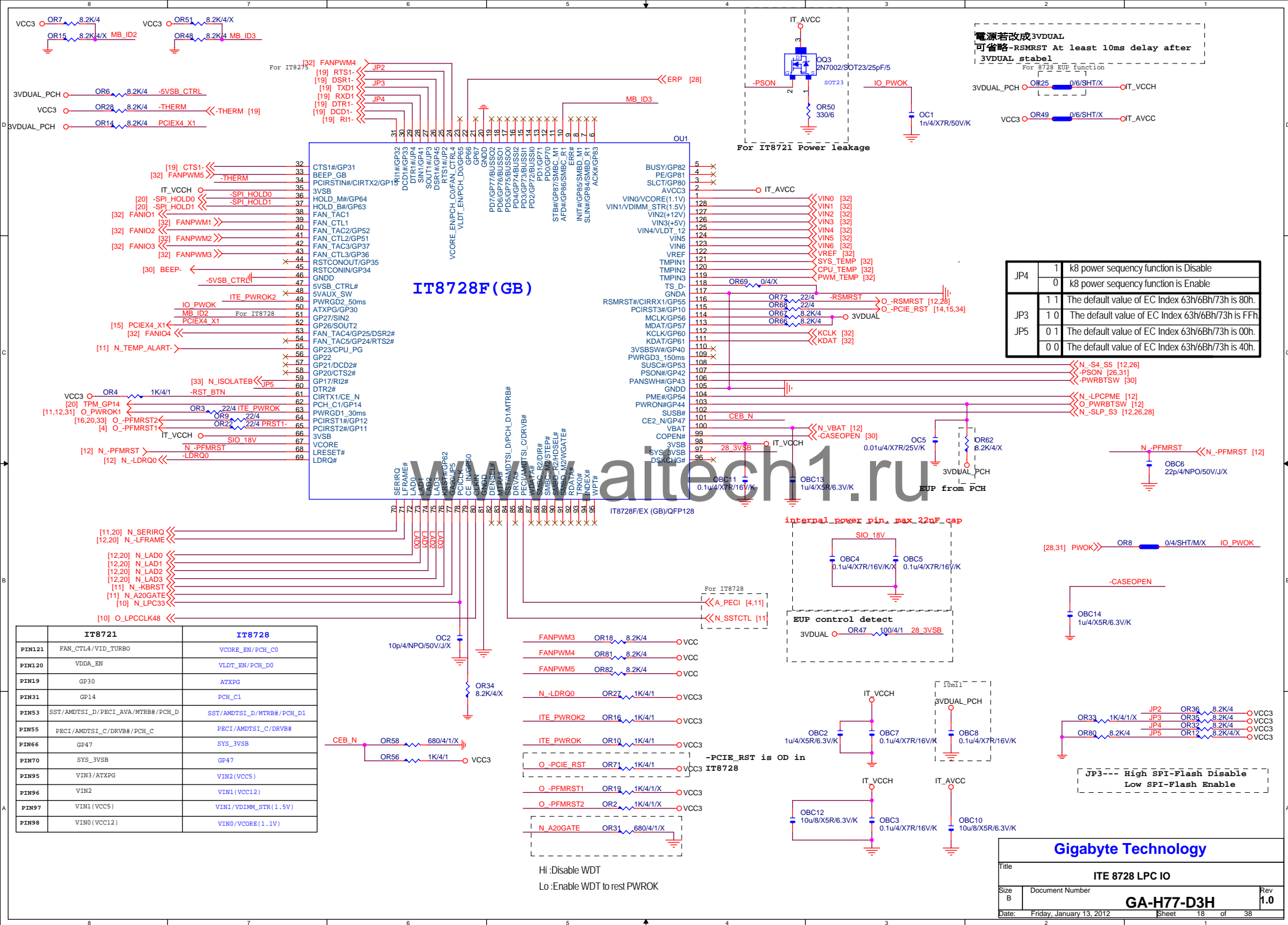
PCIE X1 1.2

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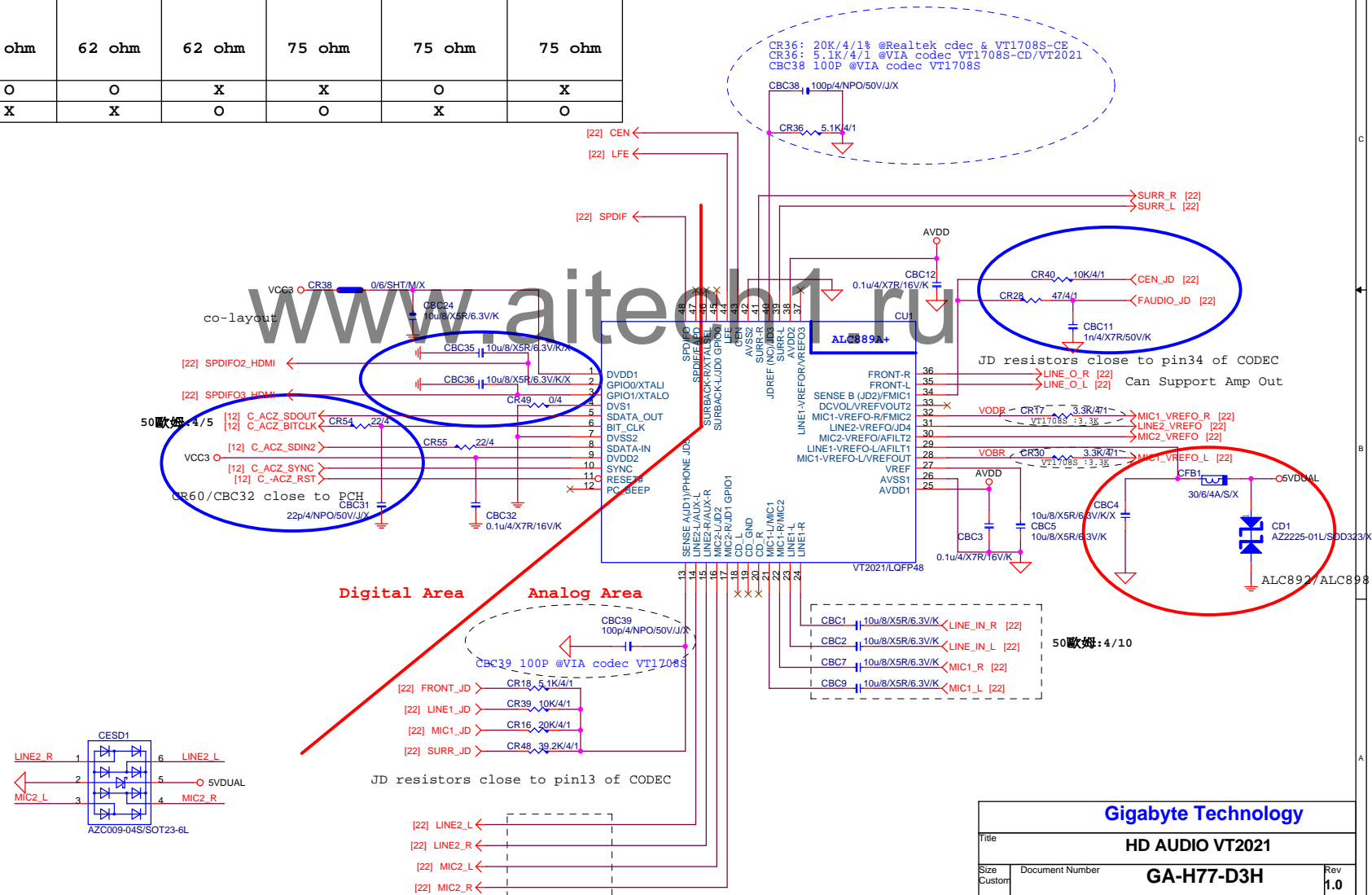






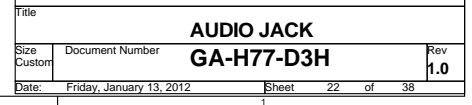
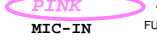
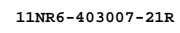


	ALC662	ALC887-VD2	ALC889	VT1708S-CD	VT1708S-CE/ VT1705CF	VT2021
CR49	X	X	O	O	X	O
CBC36	O	O	X	X	O	X
CR28/CBC11	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P	47ohm+1nF
CR52	X	O	O	O	O	O
CR57	O	X	X	X	X	X
CBC1/CBC2	10uF/X5R	10uF/X5R	22uF/X5R	10uF/X5R	10uF/X5R	10uF/X5R
CR36	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1	5.1K/4/1
CR17/CR30/ CR25/CR15/CR12/CR3/	8.2K/4	8.2K/4	8.2K/4	3.3K/4/1	3.3K/4/1	3.3K/4/1
CBC38/CBC39	X	X	X	100P/4	100P/4	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR27/CR26	22K/4	22K/4	22K/4	10K/4/1	10K/4/1	10K/4/1
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR2/CR11/ CR14/CR24	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm	75 ohm
CFB1/CD1/CBC4/CBC8	O	O	X	X	O	X
CD2/CD3/CQ3/CQ4	X	X	O	O	X	O

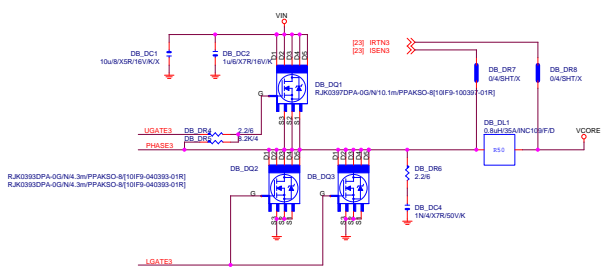


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Title			HD AUDIO VT2021
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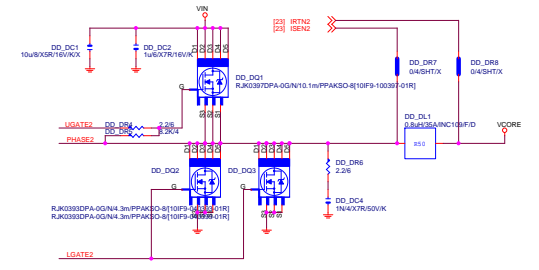




[illegible]

In Quad mode , IC1 pin10 link to IC2 pin10  
IC1 pin9 link to IC2 pin9 without PU

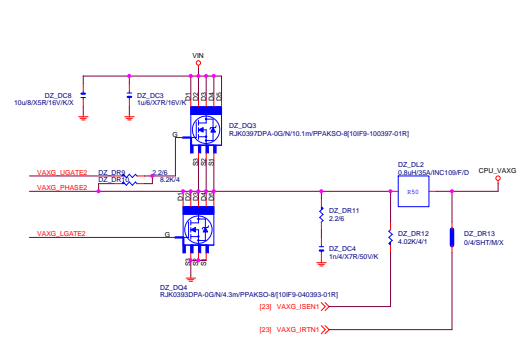
The diagram illustrates the internal DC-DC converter circuit of the TI-84 Plus CE calculator. It features a MOSFET driver (DC-DC1) and a voltage regulator (DC-DC2). The input is VCC (1.5V), and the output is VREG (5.0V). The circuit includes several capacitors (DC\_DR1, DC\_DR3, DC\_DR5, DC\_DR6, DC\_DR7) and resistors (DC\_DR2, DC\_DR4, DC\_DR8). The MOSFET driver is connected to the VCC and the DC-DC2 output. The voltage regulator is connected to the VCC and the DC-DC2 output. The output of the voltage regulator is connected to the VREG pin of the calculator.



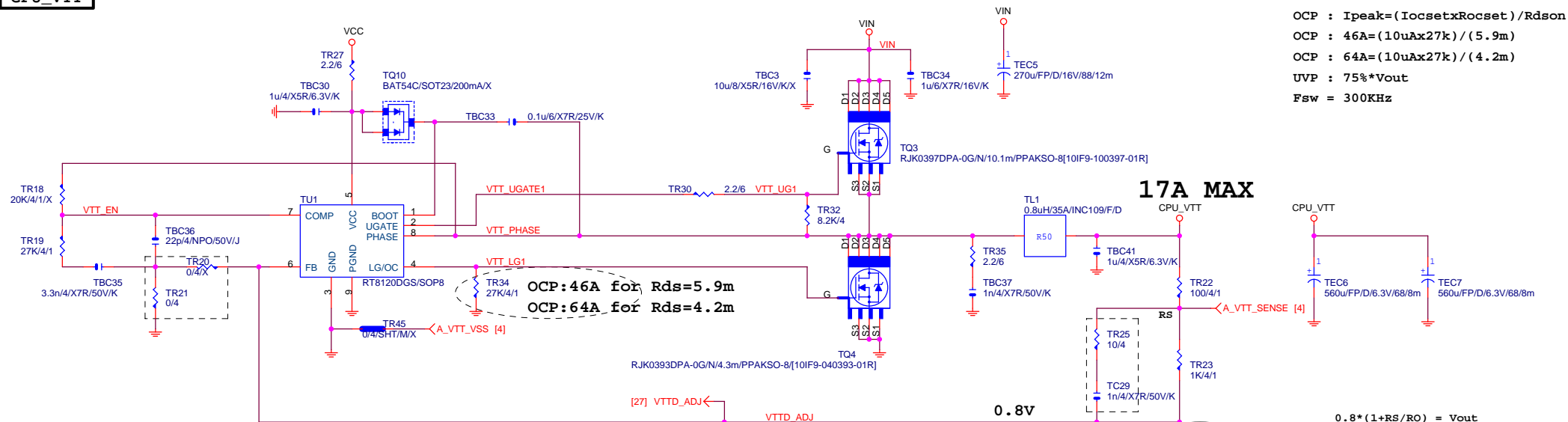
In Quad mode , IC1 pin10 link to IC2 pin10  
IC1 pin9 link to IC2 pin9 without PU

Figure 1 is a schematic diagram of the test circuit. It shows a CPU\_VAUX pin connected to two diodes, DZEC1 and DZEC2, which are connected to ground. The diodes are labeled with their specifications: 560uF/PP/D/6.3V/68/8m.

The diagram illustrates the VAXG Phase circuit. It features two 74VHC04 inverters. The first inverter's input is connected to V<sub>IN</sub> through a 10kΩ resistor (R3) and a 100nF capacitor (C1). Its output (pin 1) is connected to a 2.2kΩ resistor (R4) and a 2.2kΩ capacitor (C2), which then connects to the VAXG\_LGATE1 signal. The second inverter's input is connected to GND through a 2.2kΩ resistor (R5) and a 2.2kΩ capacitor (C3), which then connects to the VAXG\_PHASE1 signal. The output of the second inverter (pin 1) is connected to a 2.2kΩ resistor (R6) and a 2.2kΩ capacitor (C4), which then connects to the VAXG\_LGATE1 signal. The VAXG\_PHASE1 signal is also connected to a 555 timer (U1) and a CPU VAXG pin. The 555 timer is configured with its control pin to GND, its output to a 10kΩ resistor (R7) and a 100nF capacitor (C5), and its input to a 10kΩ resistor (R8) and a 100nF capacitor (C6). The CPU VAXG pin is connected to a 10kΩ resistor (R9) and a 100nF capacitor (C7).



# CPU\_VTT

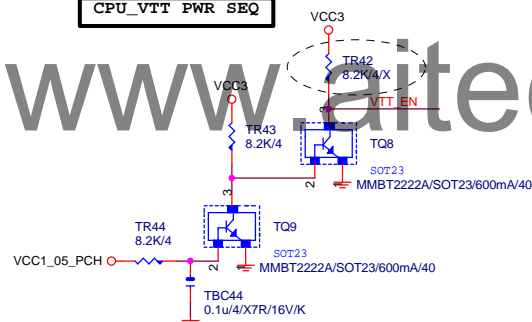


Iocset=10uA , Rocset=22k  
 OCP :  $I_{peak} = (I_{ocset} \times R_{ocset}) / R_{dson}$   
 OCP :  $46A = (10uA \times 27k) / (5.9m)$   
 OCP :  $64A = (10uA \times 27k) / (4.2m)$   
 UVP :  $75\% \times V_{out}$   
 Fsw = 300KHz

$$OCP: 46A = R_{ocset} \times I_{ocset} / R_{ds(on)}$$

$$= 27K \times 10uA / 5.9m$$

## CPU\_VTT PWR SEQ

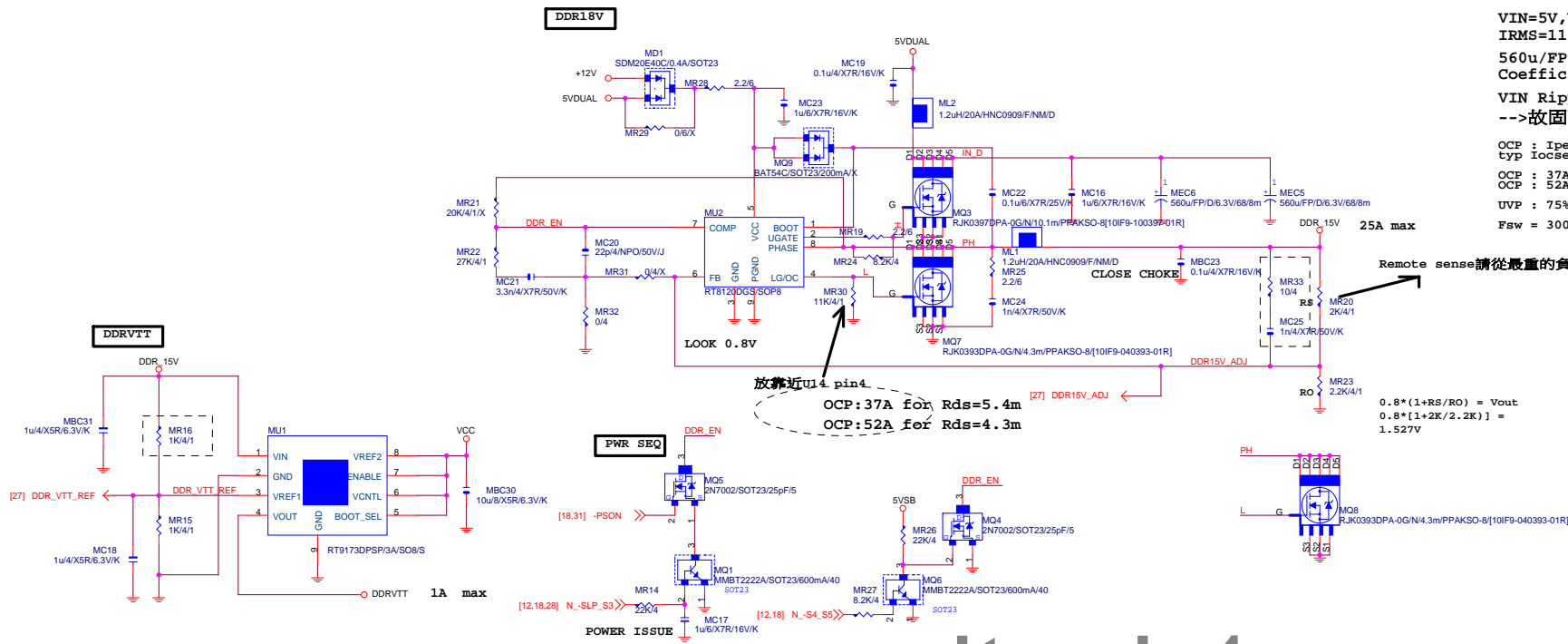


VTT_SEL	
HI	1.05V
LO	1.0V

According intel  
 CDI/IBP#476733, 固定1.05v

**GIGABYTE**

Title <b>RT8120_CPU_VTT</b>		
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VIN=5V, VOUT=1.5V, IOU=25A, PHASE=1  
 IRMS=11.45A  
 560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A  
 Coefficient=1.7(85°C), 1(105°C)  
 VIN Ripple current=4.7X1.7=7.99A(85°C)  
 -->故固態電容須2X7.99=15.98>11.45A

OCF : Ipeak=(IocsetxRocset)/Rdson  
 typ Iocset=10uA , Rocset=33k  
 OCF : 37A=(10uAx11k)/(5.9m/(5.9m))  
 OCF : 52A=(10uAx11k)/(4.2m/(4.2m))  
 UVP : 75%\*Vout  
 Fsw = 300KHz

Remote sense 請從最重的負載端點拉回

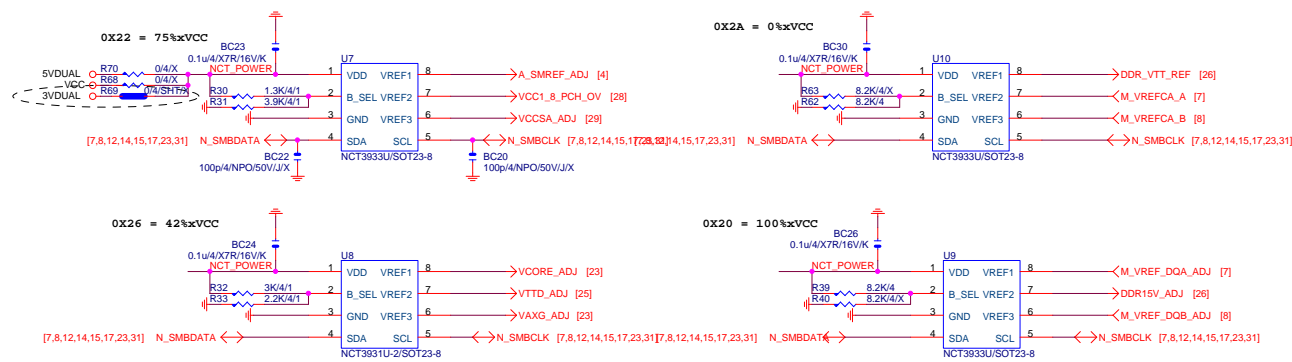
放靠近U1 pin4  
 OCF:37A for Rds=5.4m  
 OCF:52A for Rds=4.3m

0.8\*(1+RS/RO) = Vout  
 0.8\*[1+2K/2.2K] = 1.527V

GIGABYTE™			
Title			
RT8120 DDR 15V			
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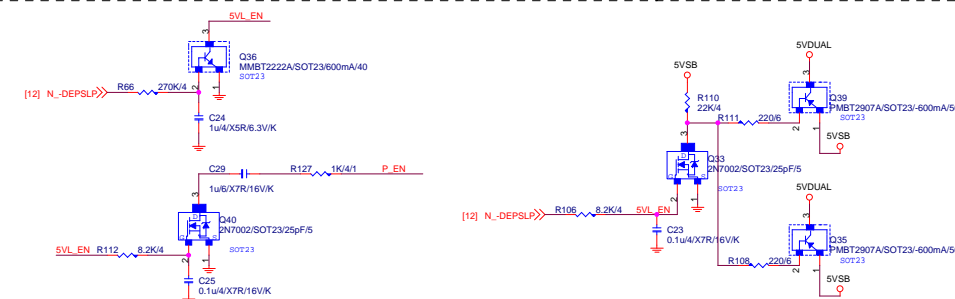
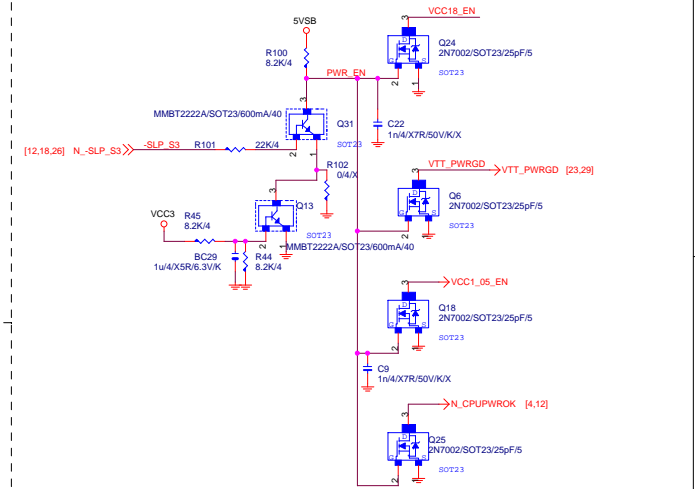
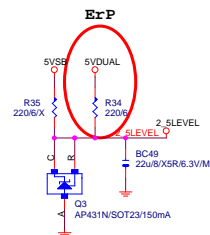
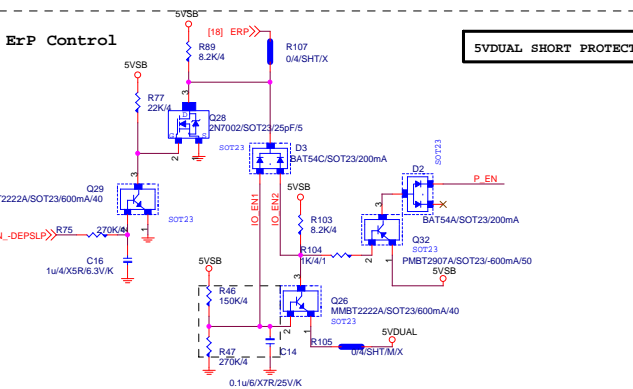
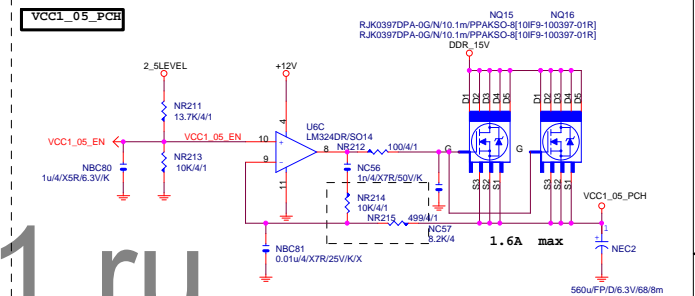
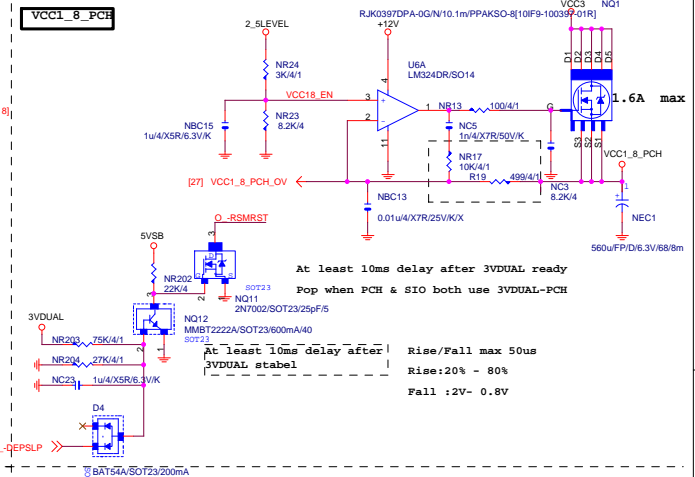
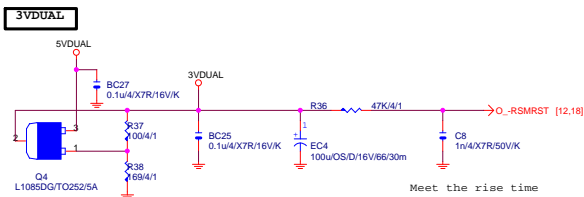
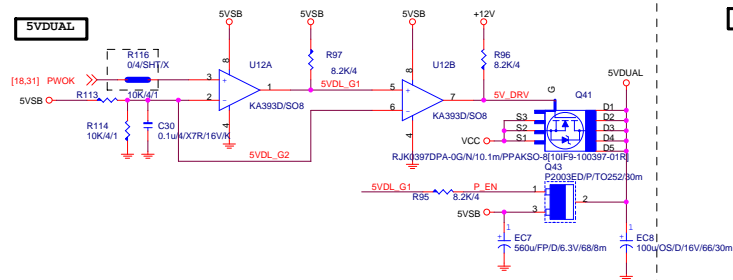


NCT3933	0X2A	0X20	0X22	0X26
VREF1	DDRVTT	VREF_DDRA_DQ	SMREF	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	CPU_VTT
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	VCCSA	VAXG

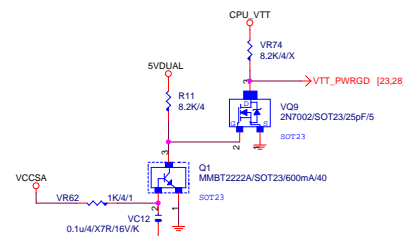
Gigabyte Technology		
Title CPU CORE VR-2		
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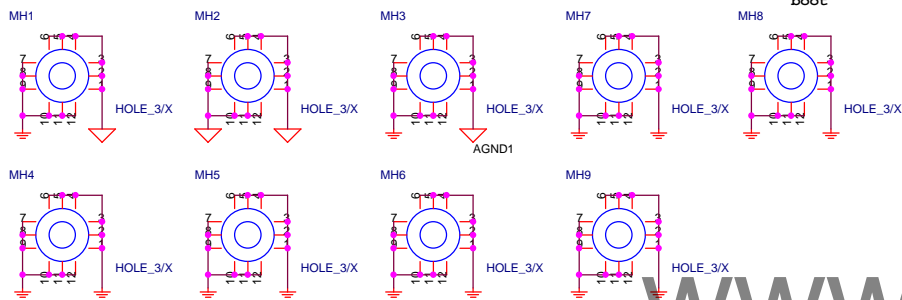
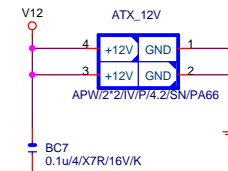
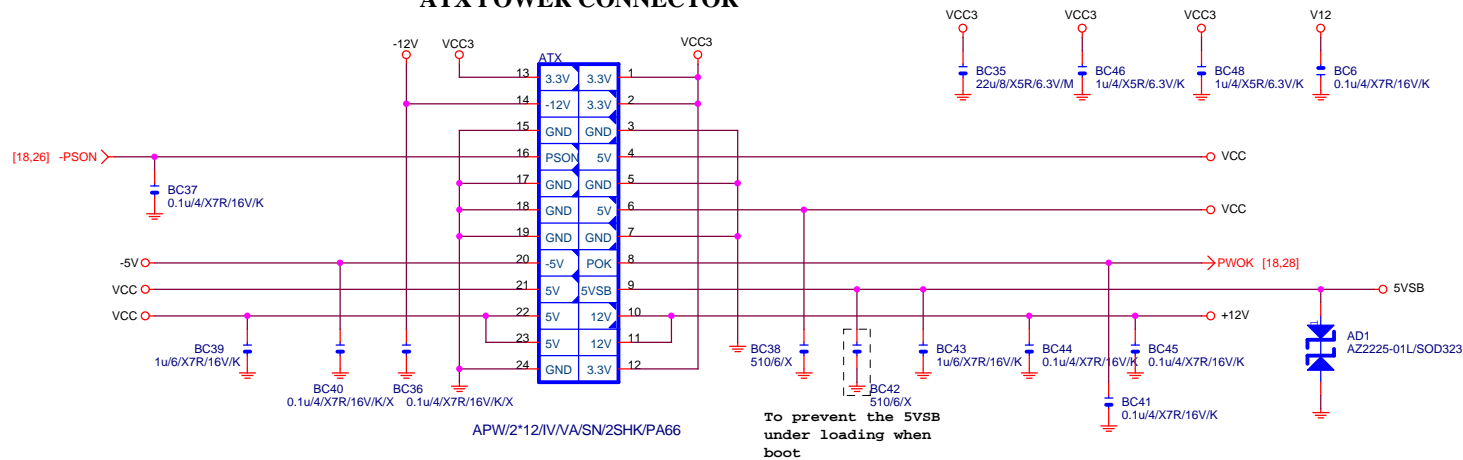


VCC\_SA



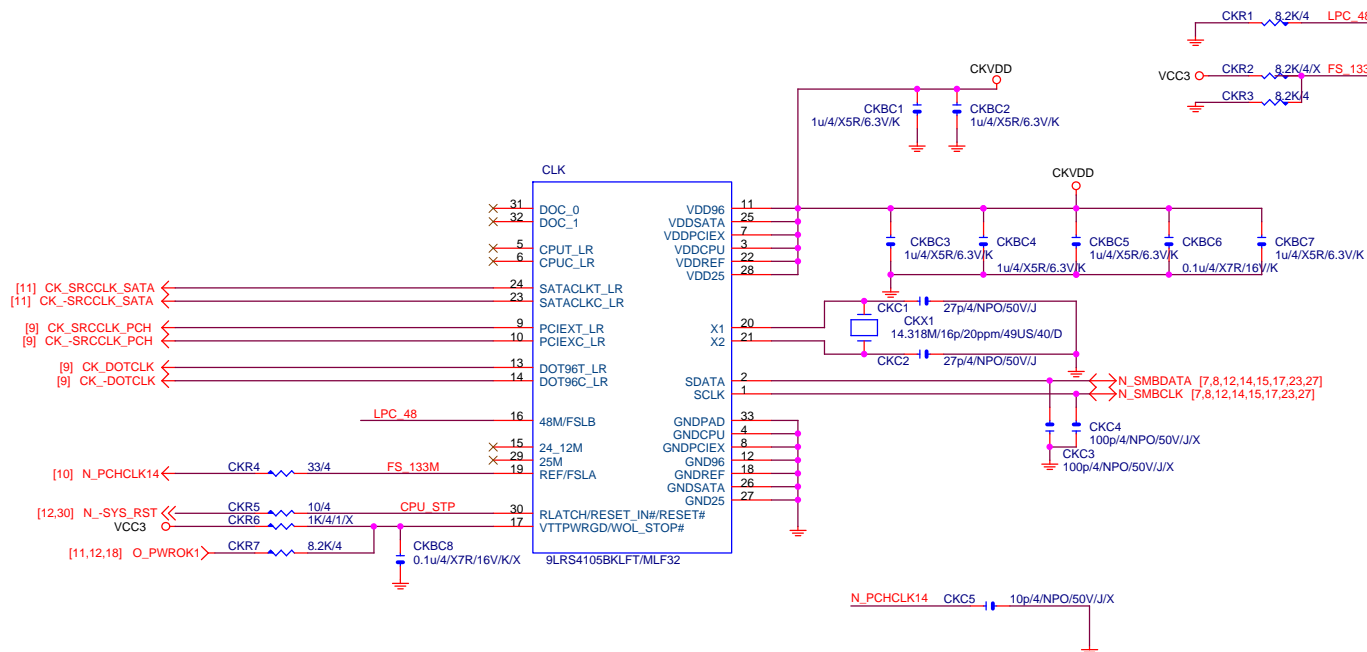


# ATX POWER CONNECTOR



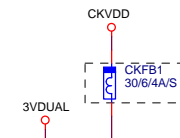
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## CLK GEN



## CPU Frequency Selection

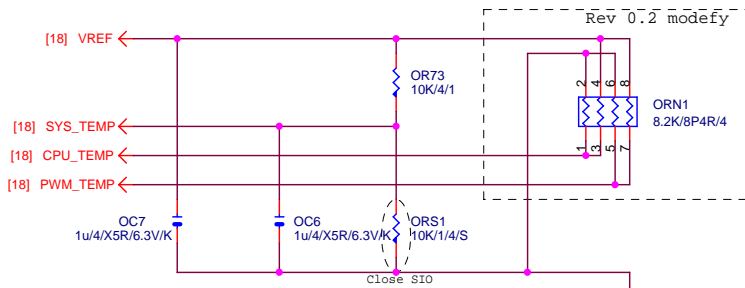
FS	CPU
0	100M <Default>
1	133M



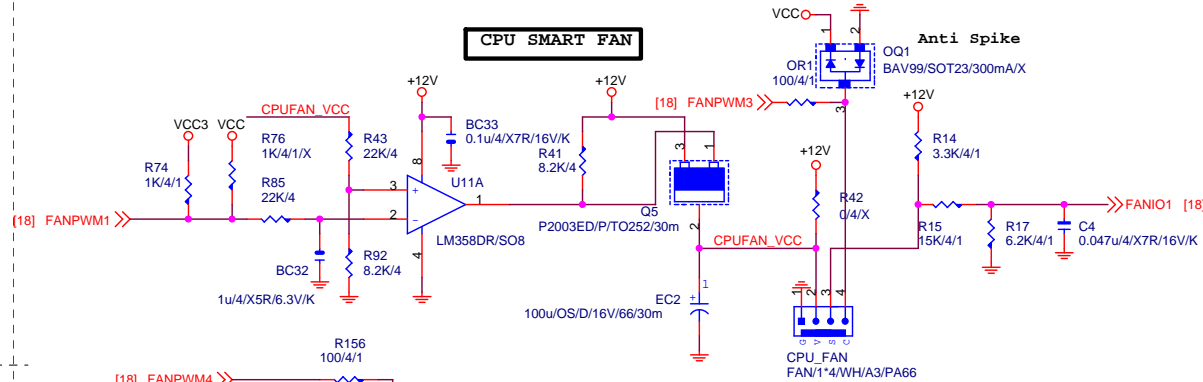
## Gigabyte Technology

Title			ATX POWER CONNECTOR
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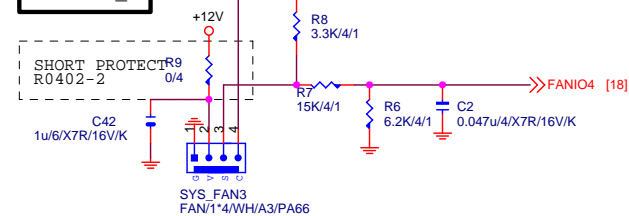
## TEMP H/W MONITOR



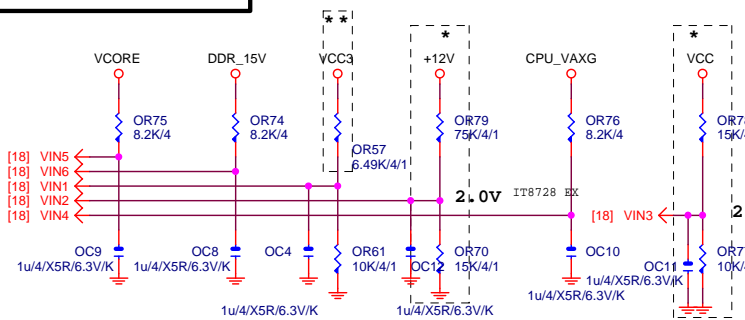
## CPU SMART FAN



## Anti Spike

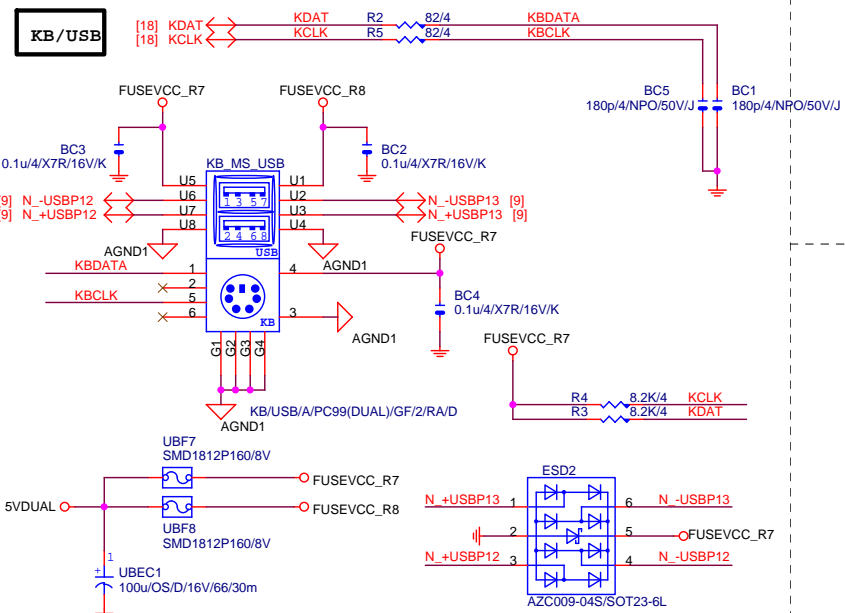


## VOLTAGE-- H/W MONITOR

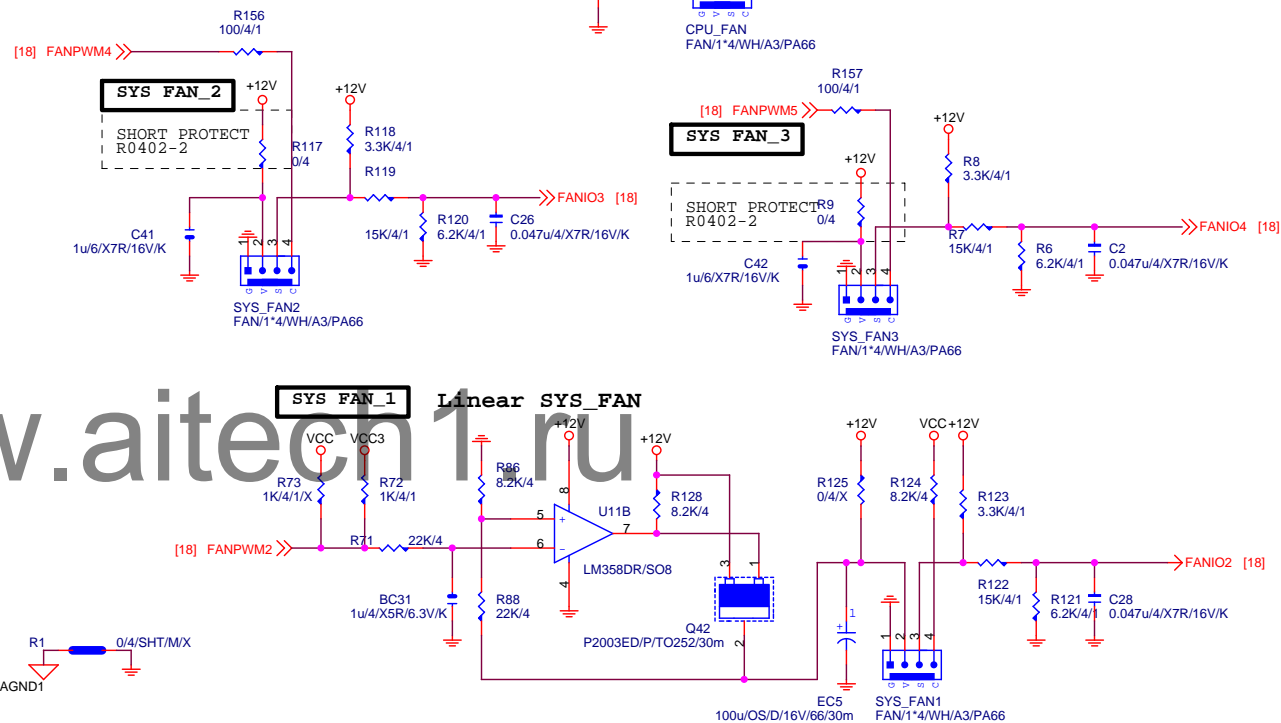


The division voltage of VIN2 & VIN3 must be around 2.9V

## KB/USB



## Linear SYS\_FAN

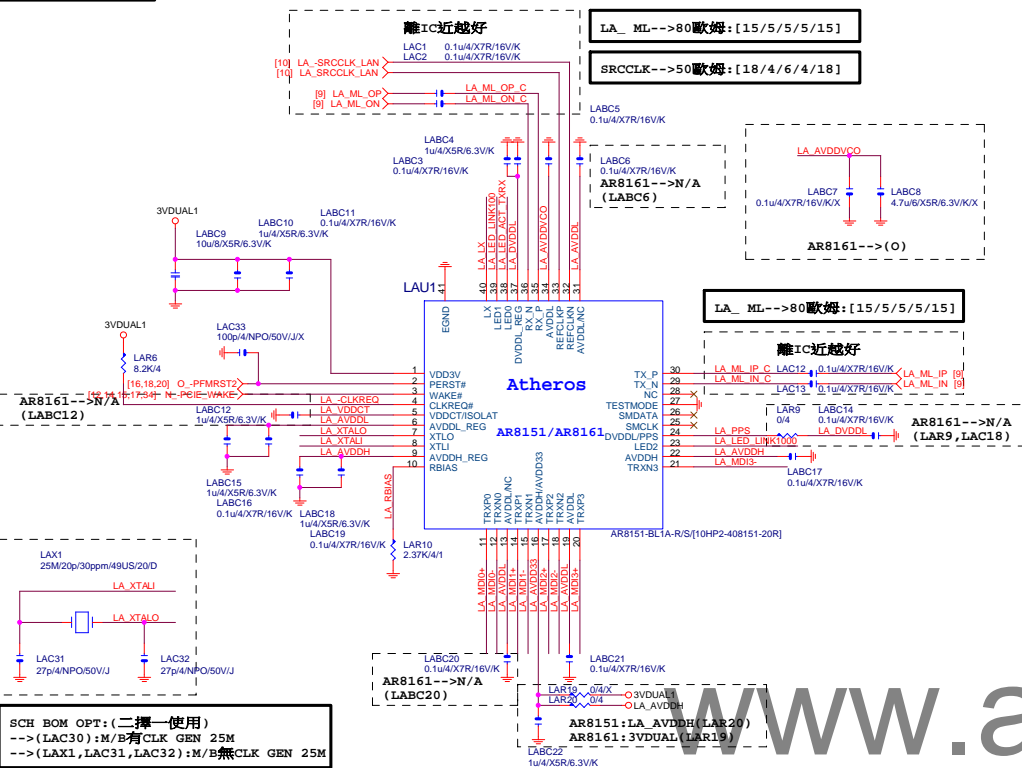


## Gigabyte Technology

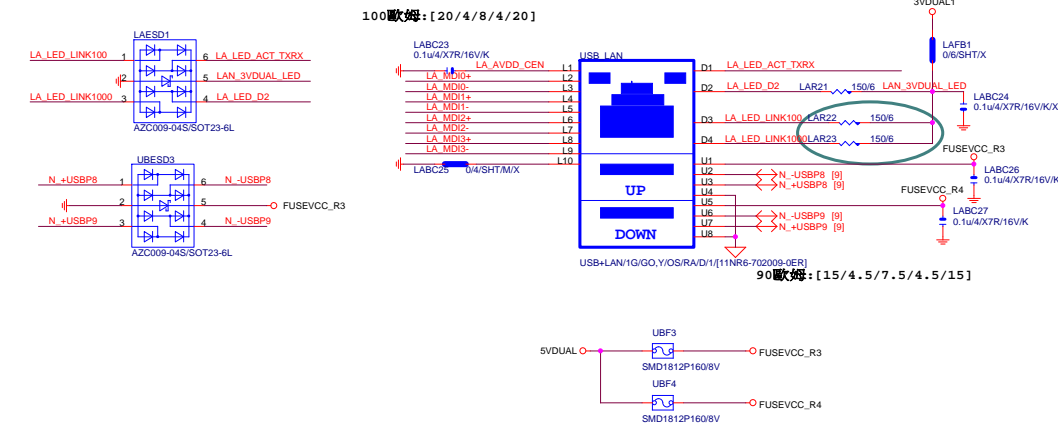
Title			
HWM,KB/MS, FAN CTRL			
Size	Document Number	Rev	
Custom	GA-H77-D3H	1.0	
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LAN:AR8151/AR8161

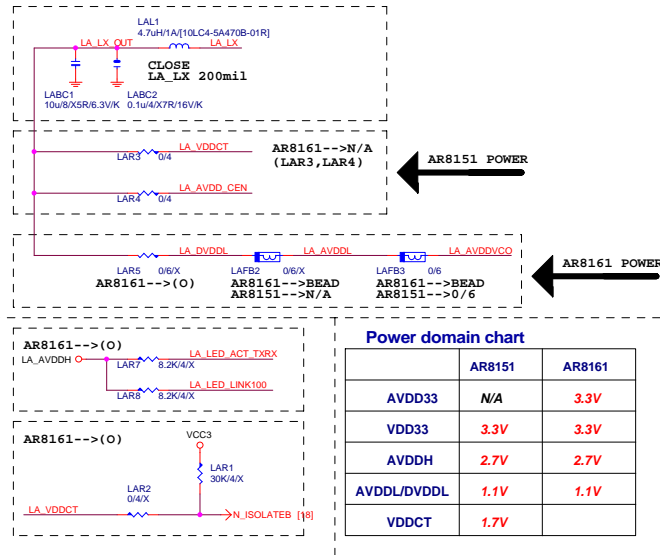


## USB30\_LAN CONNECTOR

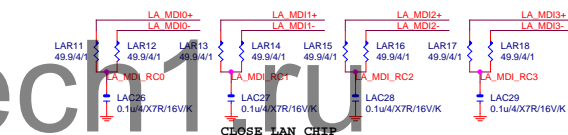


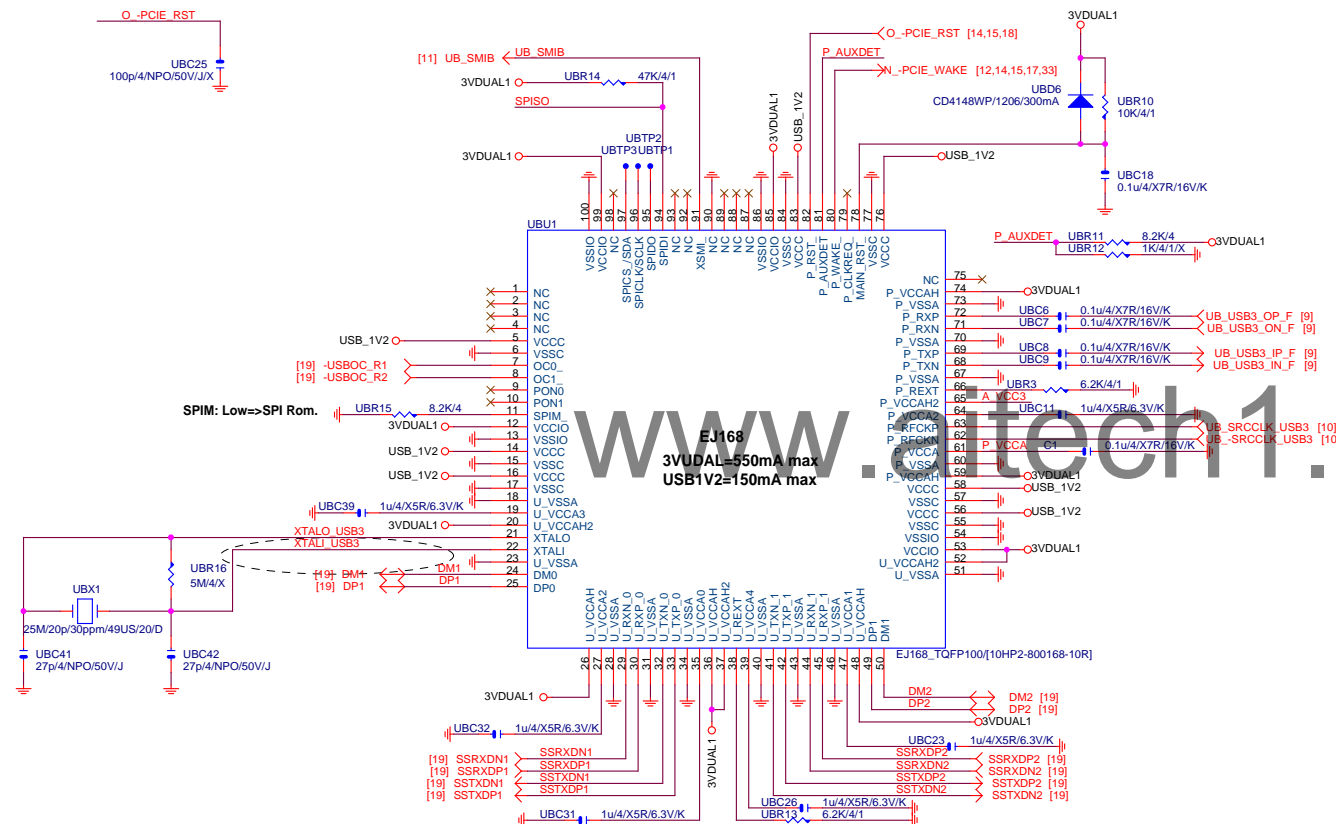
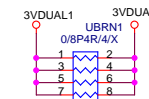
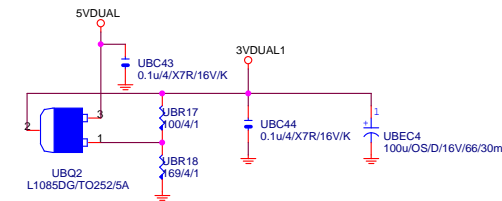
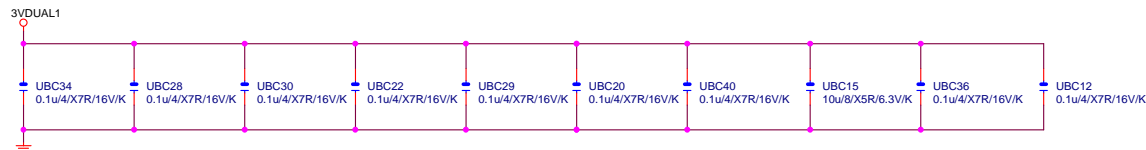
## LAN POWER

```
NEW DESIGN ONLY FOR INTERNAL SWR
AR8151:LAR3(O),LAR5(X)
AR8161:LAR5(O),LAR3/LAR4(X)
```

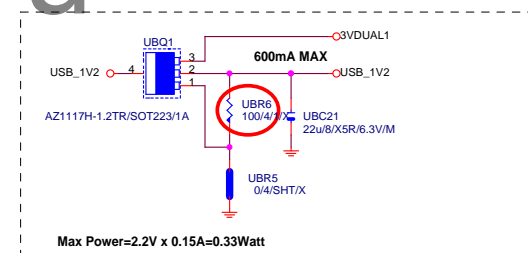


MDI : AR8161--&gt;N/A

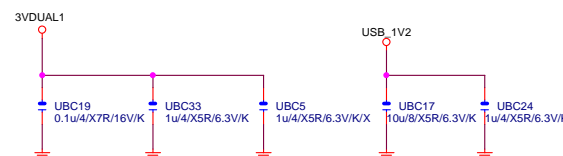
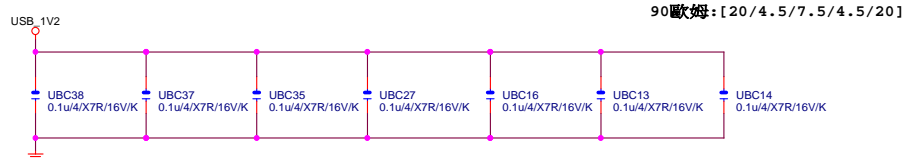




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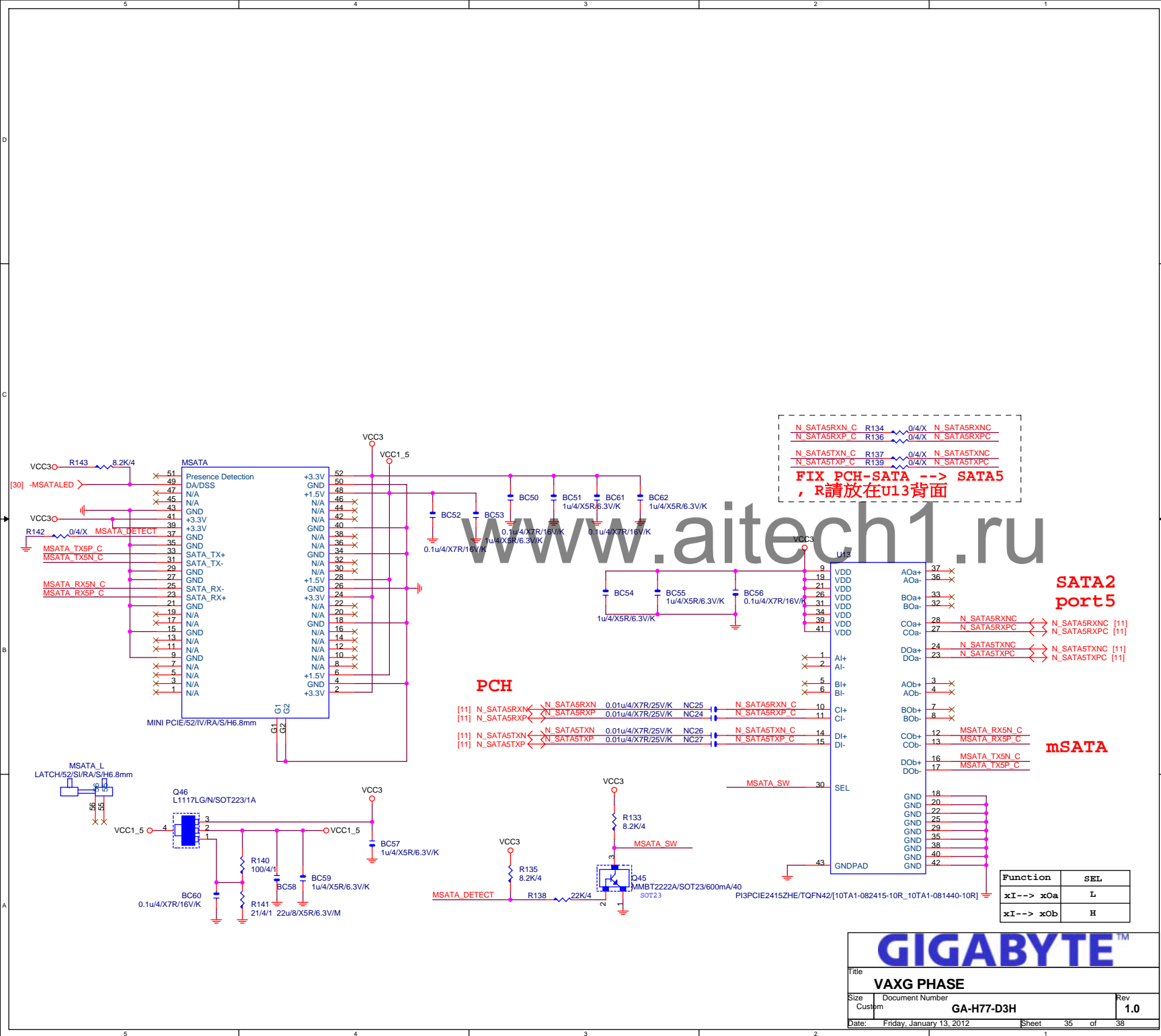


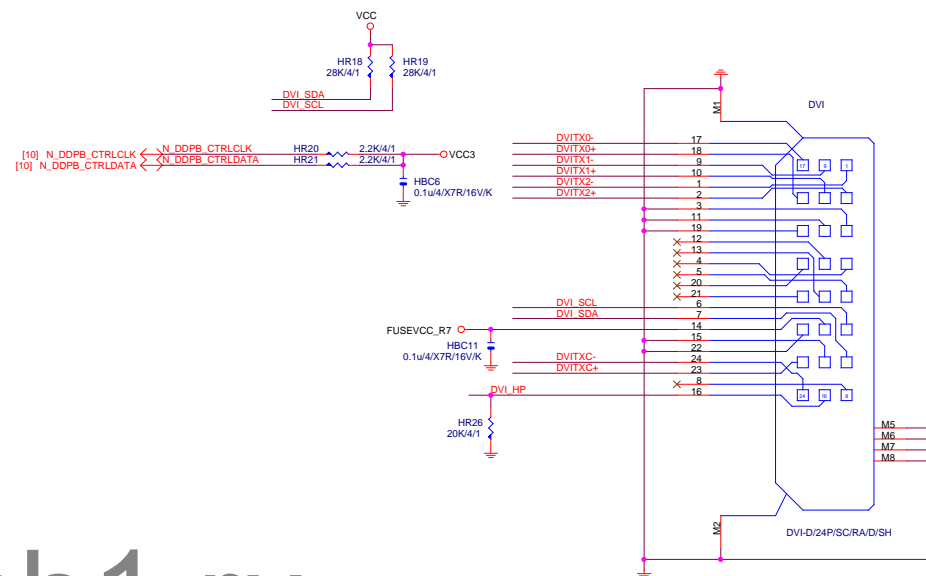
Max Power=2.2V x 0.15A=0.33Watt  
AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]  
L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]



USB3.0 --> 5GHz  
BANDWITH=5GHz\*(8b/10b)=4Gb/s=500MB/s

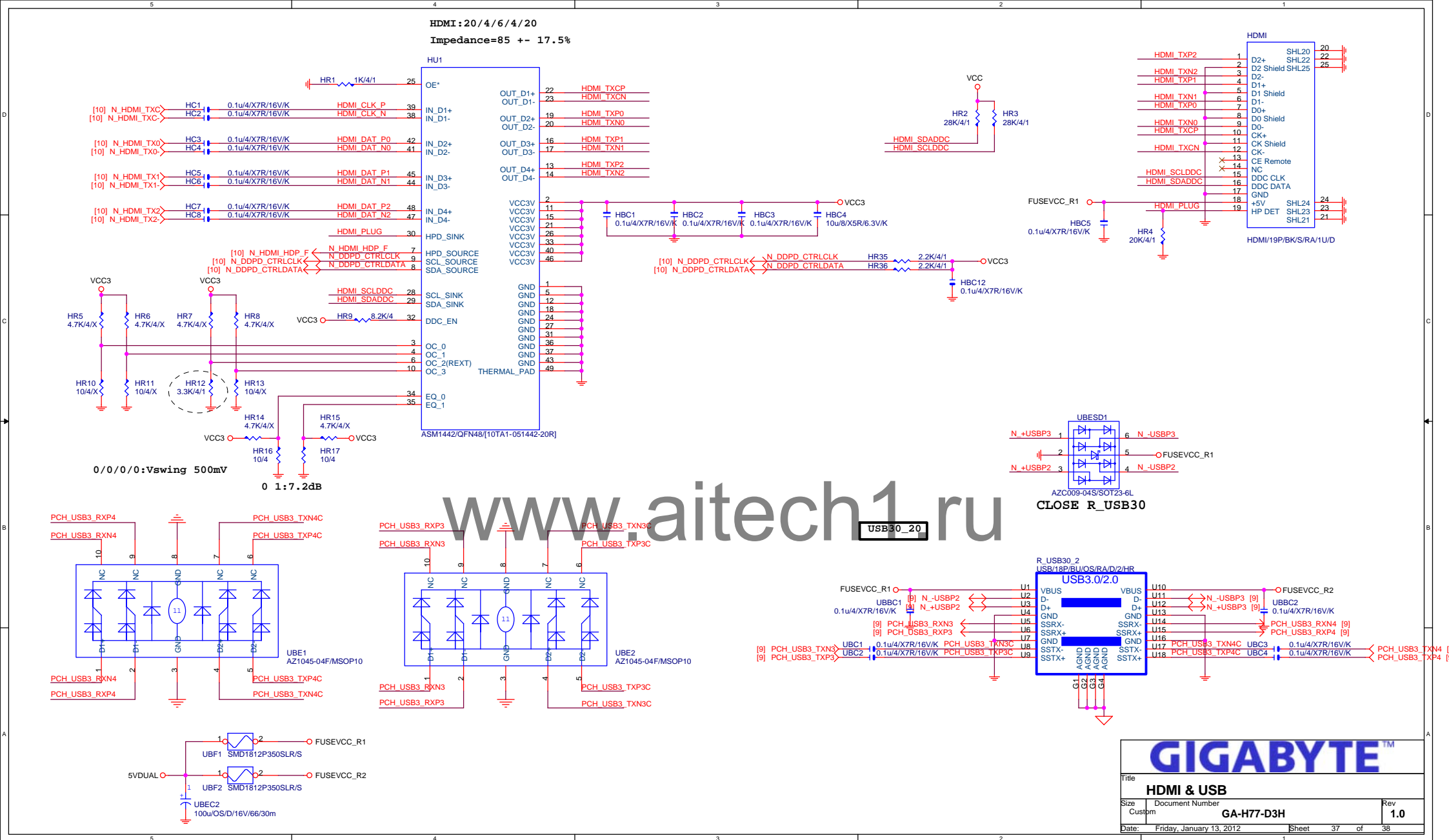
GIGABYTE™		
Title E-TRON EJ168		
Size	Document Number	Rev
Custom	GA-H77-D3H	1.0
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<i><b>Gigabyte Technology</b></i>			
Title			
<b>TI TSB43AB23 1394</b>			
Size Custom	Document Number		Rev
	<b>GA-H77-D3H</b>		<b>1.0</b>
Date:	Friday, January 13, 2012	Sheet	36 of 38



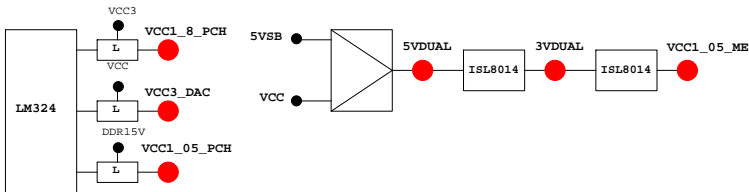
PCH GPIO LIST TABLE

PIN NAME	PWR	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI -PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI -PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE OC5#	N/A
GP10/OC6#	STBY		NATIVE OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE OC7#	N/A
GP15	STBY	L	GPO GPIO15	N/A
GP16	MAIN		GPI -SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI GPIO29	N/A
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE OC1#	N/A
GP41	STBY		NATIVE OC2#	N/A
GP42	STBY		NATIVE OC3#	N/A
GP43	STBY		NATIVE OC4#	N/A
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE -GNT1	N/A
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE -GNT2	N/A
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE -GNT3	N/A
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE -SUSTAT	N/A
GP62	STBY	L	NATIVE SUSCLK	N/A
GP63	STBY	L	NATIVE GPIO63	N/A
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL

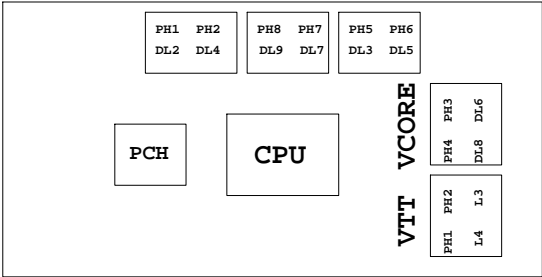
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCX	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	2X PIN	FST_2X8
INIT#/GP85/SMBC_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBC_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

散熱模組料號：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
File	TABLE LIST		
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